TECHNICAL MANUAL

COMBINED SERVICE, CIRCUIT DIAGRAMS, AND ILLUSTRATED PARTS BREAKDOWN FOR

CONTROL-MONITOR GROUP OK-145/TSC-60(V)

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(COLLINS RADIO COMPANY)
F19628-68-C-0164

(J.A. Niland & Associates Inc.)
F04606-75-D-0092

(ROCKWELL INTERNATIONAL)
(COLLINS TELECOMMUNICATIONS SYSTEMS DIVISION)
F04606-79-C-0473

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(Prefix each reference number with the chapter number denoted by the column.)

(KEY: Numbers preceded by f are illustrations; t are tables; others are paragraphs.)

OFFICIAL NOMENCLATURE COMMON NAME	CHAPTER 2 INSTALLATION	CHAPTER 3 OPERATION	CHAPTER 4 PRINCIPLES OF OPERATION	CHAPTER 6 ILLUSTRATED PARTS BREAKDOWN	CHAPTER 7 CIRCUIT DIAGRAMS
Accessible memory card	--	--	10, 35, 91, f1	f8	f6
Agc amplifier	--	--	38, 139, f1	f11	f12
Audio control card	--	--	139	f12	f12
Backplane card	--	--	28, 72, f1	f2, f10	f4
CCCS timing card	--	--	10, 116, f1	f5	f9
Control-Monitor C-8364/TSC-60(V) Audio control unit	--	f1, t3	7, 36, 137, f1	f11	f12, t7
Control-Monitor OK-145/ TSC-60(V) Radio control group	1 thru 22, t1	1 thru 13, f1, t1, t2, t3	1 thru 143, f1 thru f3, t1 thru t11	f1 thru f11	f1 thru f12, t1 thru t7
Control, Receiver C-8362/TSC-60(V) Receive control head	22	f1, t2	6, 27, 54, 132, 140, f1, t1, t3, t11	f10	f2, t1 thru 3
Control, Transmitter C-8363/TSC-60(V) Transmit control head	22	f1, t1	4, 27, 54, 132, 140, f1, t2, t3, t11	f2	f1, t4 thru t6
Hardwire memory card	--	--	31, 111, f1	f4, f4A	f8, f8A
Instruction decode card	--	--	34, 102, f1	f7	f7

CROSS-REFERENCE INDEX (Cont)

(Prefix each reference number with the chapter number denoted by the column.)

(KEY: Numbers preceded by f are illustrations; t are tables, others are paragraphs.)

OFFICIAL NOMENCLATURE COMMON NAME	CHAPTER 2 INSTALLATION	CHAPTER 3 OPERATION	CHAPTER 4 PRINCIPLES OF OPERATION	CHAPTER 6 ILLUSTRATED PARTS BREAKDOWN	CHAPTER 7 CIRCUIT DIAGRAMS
Line amplifier	--	--	36, 137, f1	f11	f12
Logic level slave card	--	--	30, 74, f1	f3	f5
Matrix card	--	--	29, 62, f1	f9	f3
Mike amplifier	--	--	36, 137, f1	f11	f12
Processor card	--	--	33, 125, f1	f6	f10
Receive control head front panel	--	f1, t2	6, 27, 54, f1	f10	f2, t1
Receive control head rear panel	--	--	6, f1	f10	t2, t3
Speaker amplifier	--	--	36, 137, f1	f11	f12
Transmit control head front panel	--	f1, t1	4, 27, 44, f1	f2	f1, t4
Transmit control head rear panel	--	--	6, f1	f2	t5, t6

CONFIGURATION STATUS PAGE

The latest configuration identifiers (CI) and alphabetic identifiers covered by this technical order are listed below with the units and subassemblies that compose Control-Monitor Group OK-145/TSC-60(V). Refer to the introduction for an explanation of the configuration status.

UNIT/SUBASSEMBLY	COLLINS PART NUMBER	LATEST CI EFFECTIVITY	LATEST ALPHABETIC EFFECTIVITY
Control-Monitor Group OK-145/TSC-60(V)	789-7497-001		B
Control Transmitter C-8363/TSC-60(V)	787-6487-001	CI-73037	AA
A7A1	793-9260-001	CI-72405	AN
A7A2	789-2620-001	CI-72266	AN
A7A2	633-9332-001	None	D
A7A3	789-2618-001	CI-72266	AE
A7A4	789-2622-001	CI-72266	AG
A7A5	789-2624-001	CI-72266	AB
A7A6	793-8982-001	CI-73033	BF
A7A7	789-2612-001	CI-72283	AF
A7A8	789-2626-001	CI-72333	P
A7A9	789-2594-001	CI-72357	M
A7A10	789-2596-001	CI-72357	R
A7A10PS1	793-9305-001	CI-72077	J
A7A10PS1A1	793-9321-001	CI-72266	U
A7A10PS1A2	793-9322-001	CI-72283	AF
Control, Receiver C-8362/TSC-60(V)	787-6444-001	CI-72357	Y
A8A1	793-9260-001	CI-72405	AN
A8A2	789-2612-001	CI-72283	AF
A8A3	789-2626-001	CI-72333	P
A8A4	789-2591-001	CI-72357	L
A8A5	789-2593-001	CI-72357	R
A8A5PS1	793-9305-001	CI-72077	J
A8A5PS1A1	793-9321-001	CI-72266	U
A8A5PS1A2	793-9322-001	CI-72283	AF
Control-Monitor C-8364/TSC-60(V)	789-8117-001	CI-72477	AU
A1	783-1427-001	CI-72266	K

INTRODUCTION

Control-Monitor Group OK-145/TSC-60(V) is an equipment that uses serial, digital information for complete control and monitoring of radio equipment with a minimum number of interconnections. For simplicity, the equipment is called radio control group throughout this technical manual. Each radio control group provides independent operational control and status monitoring of a high-frequency (hf) transmitter-receiver set that includes an exciter, a power amplifier, a coupler, a receiver, and a maintenance display.

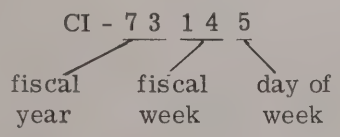
This manual is a combined service, circuit diagram, and illustrated parts list manual that contains information pertaining to the operation of the equipment and subassemblies. Information provided is divided into seven chapters as follows: Chapter 1, General Information; Chapter 2, Installation; Chapter 3, Operation; Chapter 4, Principles of Operation; Chapter 5, Maintenance; Chapter 6, Illustrated Parts Breakdown; and Chapter 7, Circuit Diagrams.

Applicable publications governing the format, use of abbreviations, symbols, and reference designations used in this manual are as follows:

MIL-T-9941	Technical Manuals: Ground C-E Equipment, Facility, Site and System, Preparation of
MIL-M-38730 (Amendment 1)	Manuals, Technical: General Requirements for Preparation of
MIL-STD-12C	Military Standard Abbreviations for use on Drawings, Specifications, Standards, and in Technical Documents
MIL-M-8910 (Amendment 1)	Technical Manuals: Illustrated Parts Breakdown, Preparation of
MIL-STD-15-1A	Graphical Symbols for Electrical and Electronic Diagrams
ASA Y32, 16-1965	Electrical and Electronic Reference Designations
MIL-STD-806B	Military Standard Graphic Symbols for Logic Diagrams

Refer to T. O. 00-25-234 for instructions concerning procedures and specific materials to be used when soldering components in this equipment.

There are two methods of identifying the configuration status of the units and subassemblies described in this technical order. One method uses a 5-digit number that is called a configuration identifier (CI). A typical 5-digit CI is constructed as follows:



When a process, electrical or mechanical change is made on a unit or subassembly, the CI is also changed. For example: If the configuration status of a unit or subassembly is changed on the fifth day of the fourteenth week of fiscal year 1973, the CI stamped on new units or subassemblies is CI-73145.

When possible, the CI number is marked on the unit or subassembly approximately two spaces following the 10-digit part number. If this is not possible, the CI is located as close to the part number as possible. On circuit cards that have a high density of parts, the part number may be located on one side of the card and the CI on the other side.

NOTE

If two or more CI numbers appear on a unit or subassembly, the CI with the latest date reflects the configuration status.

The second method of identifying configuration status uses an alphabetic identifier. The alphabetic identifier is preceded by the letters REV

(revision) and starts with REV-0 (zero) if no changes have been processed. The first change is identified as REV-A, the second as REV-B, continuing through REV-AA REV-AB, ... REV-BA, REV-BB, and ultimately to REV-ZZ, except that the letters I, O, Q, and X are not used individually or combined with another letter.

Some units or subassemblies may have both CI and alphabetic identifiers. In these instances, the alphabetic identifier reflects the latest configuration status.

NOTE

The CI and the alphabetic identifier are not serial numbers because several units or subassemblies may have the same configuration status.

The configuration status page preceding this introduction lists the latest configuration status for the units and subassemblies described in this technical order. In addition, the illustrated parts list in chapter 6 and the schematic diagrams in chapter 7 reflect the configuration changes that affect this documentation. Because all configuration changes do not affect the illustrated parts breakdown and/or the schematic diagrams, the CI's and alphabetic identifiers shown in chapter 6 and 7 may reflect an earlier configuration status than that shown on the configuration status page.

The following glossary defines a number of terms, nonstandard abbreviations, and mnemonics used in the preparation of this manual.

GLOSSARY

A	Accessible Memory Address 1
ACC	Accumulator Clock
ACD	Accumulator Input Bar
AL1	Monitor Storage Address 1
AL2	Monitor Storage Address 2
AL3	Monitor Storage Address 3
AL4	Monitor Storage Address 4
AME	Amplitude Modulation Equivalent
ANR	Address Shift Signal
ARC	Address Select Clock
B	Accessible Memory Address 2
BNZ + CNZ + COZ	Conditional branch test signal
BPZ	Branch Indirect Bar
$\overline{BR}$	Branch Bar
C	Accessible Memory Address 3
CA	Radio Counter State A
CB	Radio Counter State B
CCCS	Communications Computation Control System
CLL	Clock, Logic Level
COZ + BNZ + CNZ	Branch Signal
CRA	Radio Counter Address bit 1
CRB	Radio Counter Address bit 2
D	Accessible Memory Address 4
DBC	Data Bank Clock
DBI	Data Bank Input
DCFE	Device Control Functional Element
DCU	Device Control Unit
DBO	Data Bank Output
DBOT	Data Bank Output Retimed
DBT	CCCS Control Data
DELIM	Delimiter
DIA	Dialogic Reference
EA1	Address Enable 1
EA2	Address Enable 2
EA3	Address Enable 3
EA4	Address Enable 4
EA5	Address Enable 5
EA6	Address Enable 6
EA7	Address Enable 7
EA8	Address Enable 8
EEL	Logic Level Address Enable

GLOSSARY (Cont)

EMB	Accumulator Clock Enable
EXP	Expander Output
FD	Fault Register Output
FI	Fault Data In
FIC	Fault Data Clock
FINS	Fault In Instruction Register
FL	CCCS Fault Inhibit
IAC CLOCK	Instruction Address Counter Clock
IAC LOAD PULSE	Instruction Address Counter Load Pulse
IDRT	Process Time Interval Signal
IDS	Input CCCS Data Signal
INC	Instruction Storage Clock
ISB	Independent Sideband
LCD	Literal Code Signal
LL	Logic Level
LLA	Logic Level Address
LLSB	Lower Lower Sideband
MDO	Memory Data Output
OPO	Operator Output
OUTS	Output Sine Wave
PI	Power Interrupt
PTT	Push-to-Talk
Ø1	Phase 1 Clock
Ø3	Phase 3 Clock
RCT	Return Control Transfer
ROM	Read Only Memory
ROTE	Rotate Enable
RST	Reset
S1	Accumulator Output/ CCCS Subaddress 1
S2	CCCS Subaddress 2
SDT	Set for Data Transfer
SWO	Logic Level Input Bus
STR-F	Store Fault Data
SYNC (LL DELIM)	Logic Level Sync Bar
$\overline{\text{SYNC (LL DELIM)}}$	Logic Level Sync Bar
TADIL	Tactical Digital Information Links
TCSC	CCCS Timing Input
UUSB	Upper Upper Sideband
YN	Logic Level Sync Enable
Z2	Memory Address WT 1024

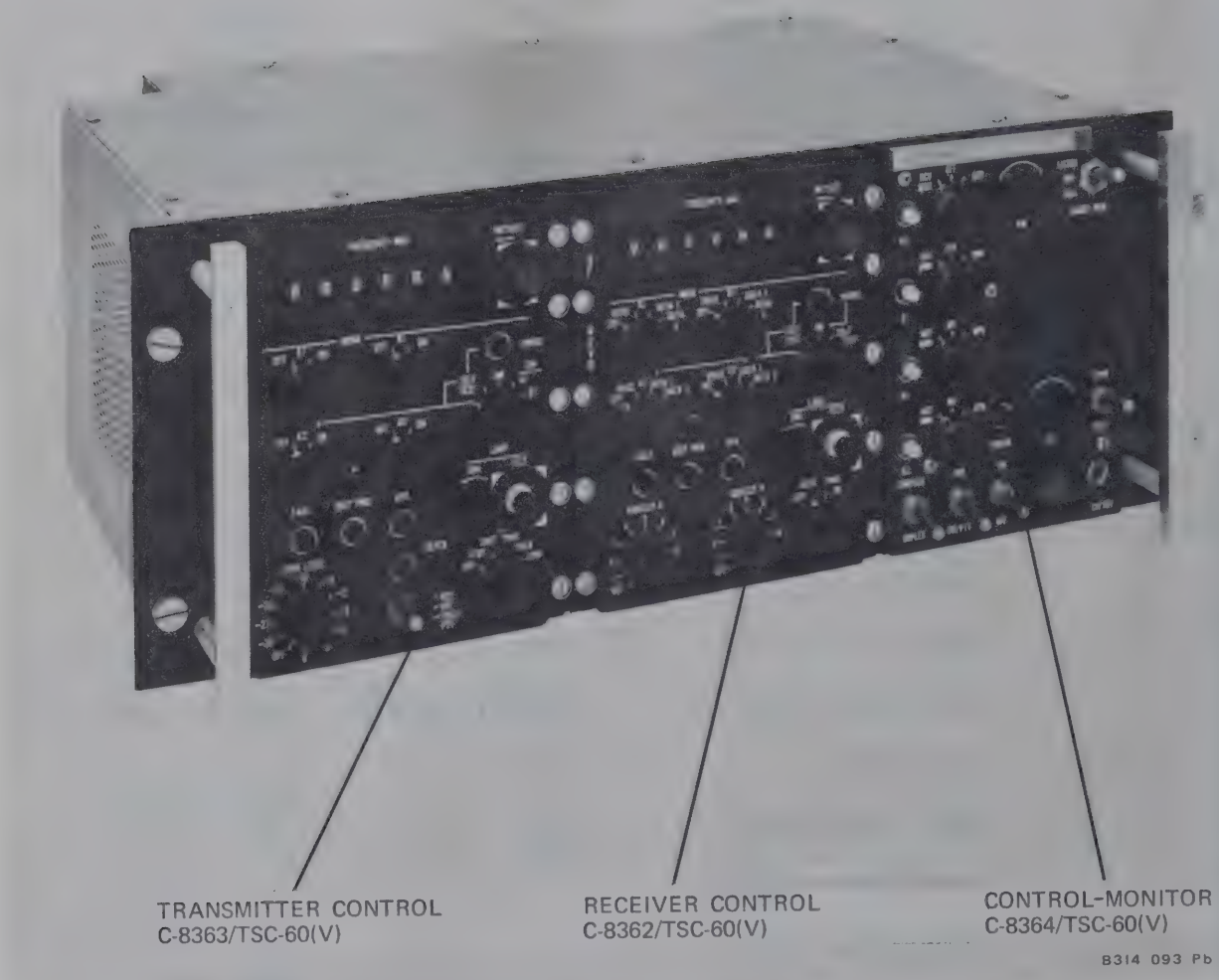


Figure 1-1. Control-Monitor Group OK-145/TSC-60(V)

CHAPTER 1

GENERAL INFORMATION

1-1. GENERAL.

1-2. This chapter contains a description of Control-Monitor Group OK-145/TSC-60(V) (radio control group) shown in figure 1-1. Tabular listings of the leading particulars, and capabilities and limitations are provided together with listings of equipment supplied and equipment required but not supplied.

1-3. DESCRIPTION AND PURPOSE.

1-4. The radio control group includes Control-Monitor C-8364/TSC-60(V) (audio control unit) figure 1-2, Transmitter Control C-8363/TSC-60(V) (transmit control head) figure 1-3, and Receiver Control C-8362/TSC-60(V) (receive control head) figure 1-4. The three units contain all the controls, indicators, and circuits required to control and operate a compatible radio transmitter and receiver set from a rack-mounted position near the radio equipment or from a remote location as far as one-quarter of a mile away. Control of the radio equipment is exercised by a read only memory (rom) computer that is part of the transmit control head. Front panel switches and indicators on the transmit and receive control heads function as a logic level interface between the computer and the radio equipment. Repositioning the front switches causes the computer to send serial digital data to the associated radio equipment. Device control units (DCU) and device control functional elements (DCFE) of the respective radio equipment act upon the serial digital data as instructed by the front panel switches and the computer program. Radio control includes such functions as frequency and mode selection, tuning, fault detection, carrier suppression, receiver squelch adjustments, and power on-off switching. After the radio equipment acts upon the instructions from the computer, the radio DCU originates a serial digital data response to the computer. This response indicates that the computer instructions were successfully completed or that a fault exists in the particular radio equipment. The computer translates the digital data information and transmits it as control instructions to the front panel indicators of the radio control group. Lighted indicators alert the operator to fault conditions or advise that the radio equipment is ready for operation. Controls on the front of the audio control unit provide facilities for audio interface with the radio equipment after it has been properly set up for operation by the transmit and receive control heads and the computer.

1-5. AUDIO CONTROL UNIT. The audio control unit (figure 1-2) is equipped to mount in a standard 19-inch equipment rack. However, the front panel occupies only 5-3/4 inches of the total width. The remainder of the front panel accommodates the transmit control head on the left and the receive control head in the center. All inputs and outputs of the unit are through a power and a signal connector on the rear of the unit. Major subassemblies of the unit include the following:

Audio control card A1 that mounts various resistors used in the audio circuits.

Audio amplifiers A2 through A6 that provide amplification of a microphone output for application to the transmit lines, and amplification of a received signal for application to either a headset or a front panel speaker.

Power supply PS1 that supplies 24 volts dc to operate the five audio amplifiers.

Filters FL1 and FL2 that filter spurious signals from the ac power circuits.

Filters FL3, FL4, and FL5 that filter spurious signals from the lines connecting the computer to the DCU's of the radio equipment.

Fan B1 that supplies cooling air for the components of the radio control group.

1-6. TRANSMIT CONTROL HEAD. The transmit control head (figure 1-3) consists of three basic assemblies: front panel A9, rear panel A10, and a center unit that includes the main chassis, a backplane card, and six perpendicular plug-in type circuit cards.

a. Front panel A9 and all the controls and indicators including the cabling unplug from

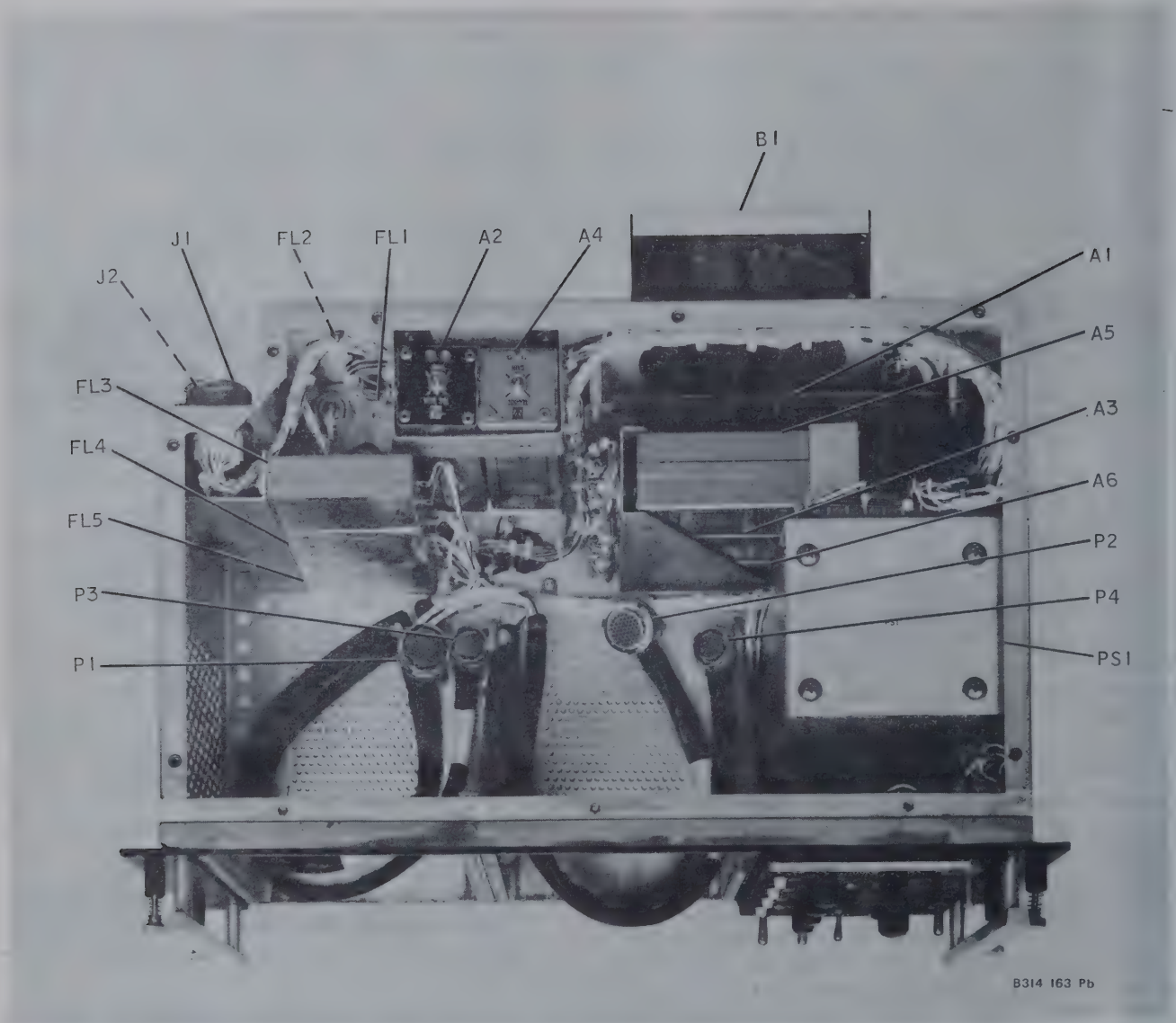


Figure 1-2. Audio Control Unit (Cover Removed)

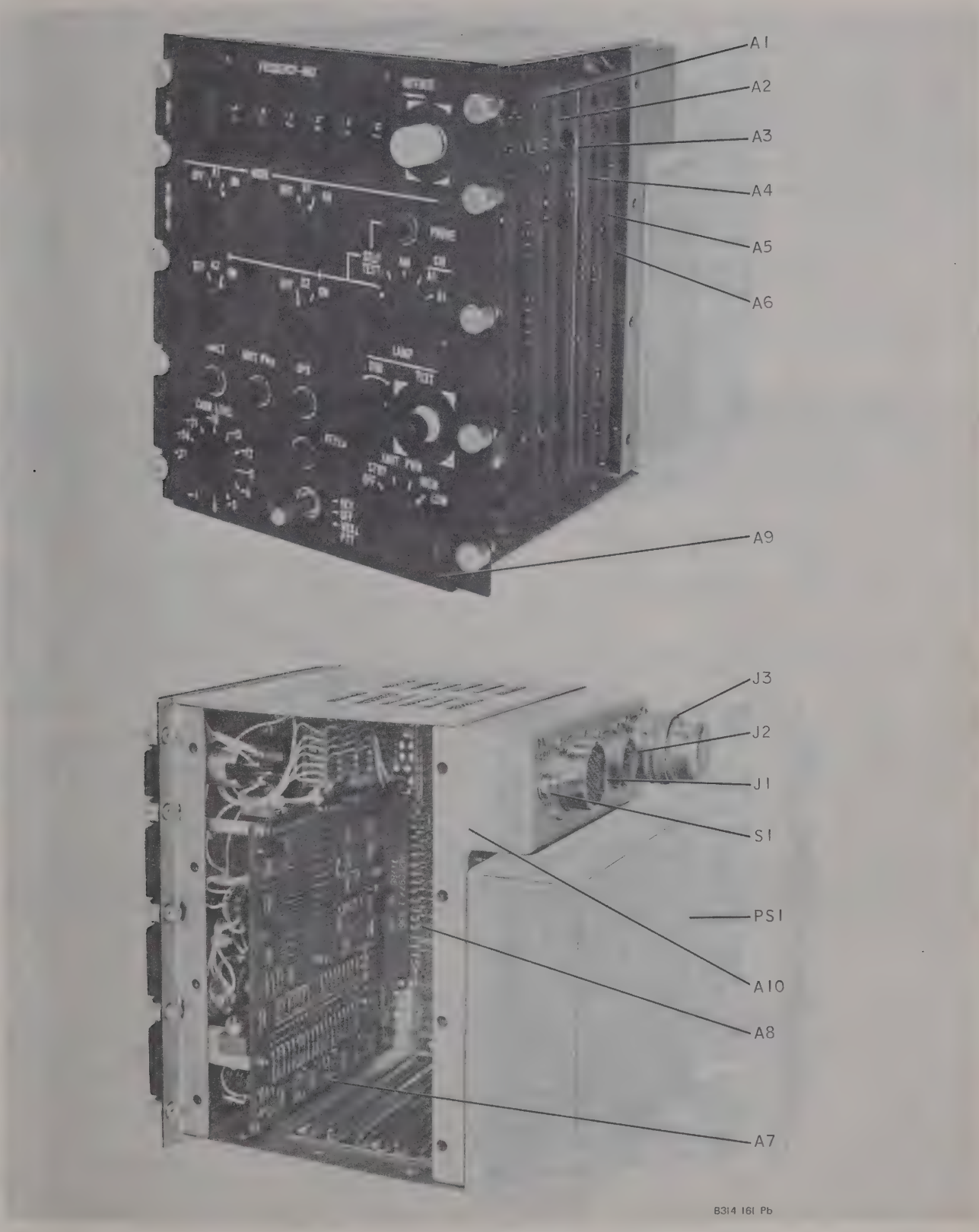


Figure 1-3. Transmit Control Head (Cover Removed)

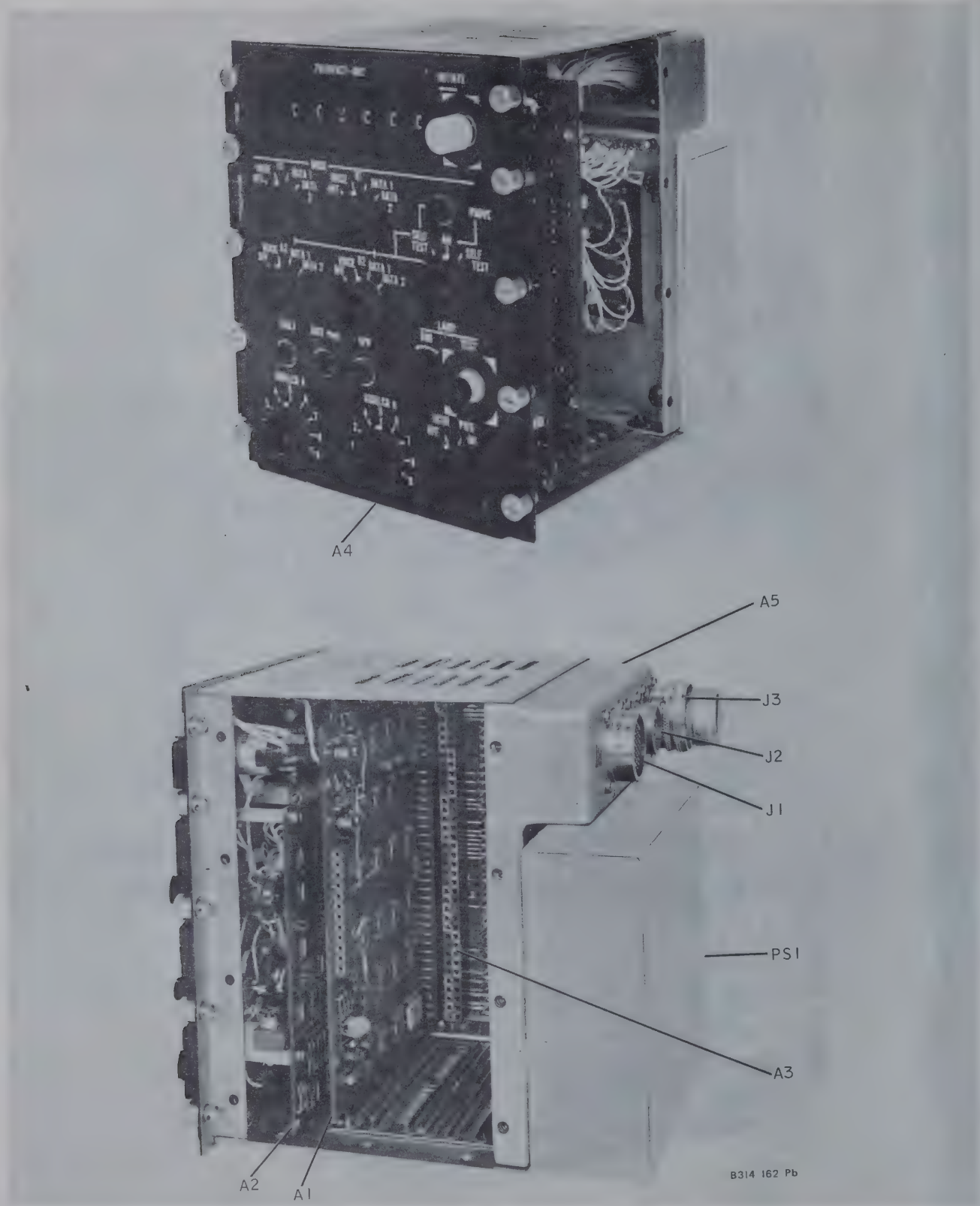


Figure 1-4. Receive Control Head (Cover Removed)

matrix card A7, which in turn plugs into backplane card A8. Front panel mounting screws secure the transmit control head in the radio control as shown in figure 1-1. Access to the circuit cards is from the side of the unit as illustrated in figure 1-3.

b. Rear panel A10 includes dc power supply PS1, three multipin connectors, and a 2-position toggle switch. Connector J1 provides the signal interface with the audio control unit, and connector J2 supplies the primary power that operates power supply PS1 and the 120-volt dimmed voltage used to light the front panel edge-lighting circuits. Connectors J1 and J2 mate with plugs P1 and P2 of the audio control unit (figure 1-2). Connector J3 (figure 1-3) provides an entry to the computer for address strapping and is equipped with a shield assembly and cover. Switch S1 is labeled PA 548U-208U and is used to select computer control of either the 548U (1-kW) or the 208U (2.5- or 10-kW) Power Amplifiers.

c. The center unit consists of the main chassis that encloses backplane card A8, logic level slave card A1, hardwire memory card A2, CCCS (communication computation control system) timing card A3, processor card A4, instruction decode card A5, accessible memory card A6, and matrix card A7.

1-7. RECEIVE CONTROL HEAD. The receive control head (figure 1-4) has the same basic construction as the transmit control head. Logic level slave card A1, matrix card A2, backplane card A3, and dc power supply PS1 are identical to those used on the transmit control head. Differences in the two control heads are primarily in the front panel switches and wiring. The receive control head is not equipped with a PA 548U-208U switch. The receive control head uses the computer in the transmit control head to control and monitor the receiving equipment.

1-8. LEADING PARTICULARS.

1-9. Table 1-1 lists the leading particulars for the audio control unit, the transmit control head, and the receive control head.

1-10. CAPABILITIES AND LIMITATIONS.

1-11. Table 1-2 lists the capabilities and limitations of the radio control group.

1-12. EQUIPMENT SUPPLIED.

1-13. Table 1-3 lists the equipment supplied with each radio control group.

1-14. EQUIPMENT REQUIRED BUT NOT SUPPLIED.

1-15. Table 1-4 lists auxiliary equipment required to operate the associated radio equipment from the radio control group, but is not supplied.

Table 1-1. Leading Particulars

CHARACTERISTIC	DESCRIPTION
AUDIO CONTROL UNIT	
Primary power requirements:	
Voltage	108 to 132 volts ac.
Frequency	47 to 62 or 380 to 420 Hz.
Phase	Single-phase.
Current	1.2 amperes, maximum including control heads.

Table 1-1. Leading Particulars (Cont)

CHARACTERISTIC	DESCRIPTION
AUDIO CONTROL UNIT (Cont)	
Dimensions:	
Height	7 in. (17.8 cm).
Width	19 in. (48.3 cm).
Depth	11 in. (27.9 cm).
Weight	24 lb (10.9 kg).
Transportability	Usually transported in equipment rack of an air or ground transportable shelter. Must be crated when shipped individually.
Storage conditions	Crated with desiccant material included.
TRANSMIT CONTROL HEAD	
Primary power requirements:	Supplied by audio control unit.
Voltage	108 to 132 volts ac.
Frequency	47 to 62 or 380 to 420 Hz.
Phase	Single-phase.
Current	0.4 ampere, maximum.
Dimensions:	
Height	6-3/4 in. (17.1 cm).
Width	5-3/4 in. (14.6 cm).
Depth	6-1/2 in. (16.5 cm).
Weight	9-1/4 lb (5.2 kg).
Transportability	Usually transported in an equipment rack of an air or ground transportable shelter. Must be crated when shipped individually.
Storage conditions	Crated with desiccant material included.

Table 1-1. Leading Particulars (Cont)

CHARACTERISTIC	DESCRIPTION
RECEIVE CONTROL HEAD	
Primary power requirements:	Supplied by audio control unit.
Voltage	108 to 132 volts ac.
Frequency	47 to 62 or 380 to 420 Hz.
Phase	Single-phase.
Current	0.4 ampere, maximum.
Dimensions:	
Height	6-3/4 in. (17.1 cm).
Width	5-3/4 in. (14.6 cm).
Depth	6-1/2 in. (16.5 cm).
Weight	9-1/4 lb (5.2 kg).
Transportability	Usually transported in an equipment rack of an air or ground transportable shelter. Must be crated when shipped individually.
Storage conditions	Crated with desiccant material included.

Table 1-2. Capabilities and Limitations

CHARACTERISTIC	DESCRIPTION
Frequency selection range	2.0000 to 29.9999 MHz in 100-Hz increments.
Orientation:	
Nonoperation and storage	Any position for a period of 2 years.
Operation	Inclination at any slope up to 10% from the normal position.

Table 1-2. Capabilities and Limitations (Cont)

CHARACTERISTIC	DESCRIPTION
Temperature range:	
Nonoperating	-62 to +71°C (-80 to +160°F).
Operating	-40 to +52°C (-40 to 125°F).
Humidity:	
Operating and nonoperating	Up to 96% with a temperature of 30°C (86°F) including condensation due to temperature change.
Altitude:	
Nonoperating and storage	Sea level to 50,000 ft (15,240 meters).
Operating	Sea level to 12,000 ft (3,658 meters).
Vibration	While mounted in the console or terminal rack, the radio control group withstands the vibration environment encountered as the communication central is subjected to the following tests on either a dolly or M-35 truck: Bounce test per method 2B of MIL-T-4807A Type III mobility test in accordance with MIL-M-008090E.
Shock	While mounted in the console or terminal rack, the radio control group withstands the shock conditions encountered as the communication central is subjected to the following shock tests: Shock per method 3C of MIL-T-4807A Helicopter landing test (simulated) 6-inch flat drop on concrete surface.
Audio line impedance:	
Transmit lines	600 ohms ±10%.
Receive lines	600 ohms ±10%, or greater than 10,000 ohms, switch selectable.

Table 1-3. Equipment Supplied

NOMENCLATURE	COMMON NAME	QTY	REFERENCE DESIGNATION
Control-Monitor Group OK-145/ TSC-60 (V) consisting of:	Radio control group		
Control-Monitor C-8364/TSC-60 (V)	Audio control unit		
Audio Control Card	Audio control card	1	A1
Line Amplifier	Line amplifier	1	A2
AGC Amplifier	Agc amplifier	1	A3
Microphone Amplifier	Mike amplifier	1	A4
Line Amplifier	Line amplifier	1	A5
Speaker Amplifier	Speaker amplifier	1	A6
Control, Transmitter C-8363/ TSC-60 (V)	Transmit control head	1	A7
Logic Level Slave Printed Circuit Board	Logic level slave card	1	A7A1
Hardwire Memory Printed Circuit Board	Hardwire memory card	1	A7A2
CCCS Timing Printed Circuit Board	CCCS timing card	1	A7A3
Processor Printed Circuit Board	Processor card	1	A7A4
Instruction Decode Printed Circuit Board	Instruction decode card	1	A7A5
Accessible Memory Printed Circuit Board	Accessible memory card	1	A7A6
Matrix Printed Circuit Board	Matrix card	1	A7A7
Backplane Printed Circuit Board	Backplane card	1	A7A8
Front Panel Assembly	Front panel	1	A7A9
Rear Panel Assembly	Rear panel	1	A7A10

Table 1-3. Equipment Supplied (Cont)

NOMENCLATURE	COMMON NAME	QTY	REFERENCE DESIGNATION
Control, Receiver C-8362/ TSC-60 (V)	Receive control head	1	A8
Logic Level Slave Printed Circuit Board	Logic level slave card	1	A8A1
Matrix Printed Circuit Board	Matrix card	1	A8A2
Backplane Printed Circuit Board	Backplane card	1	A8A3
Front Panel Assembly	Front panel	1	A8A4
Rear Panel Assembly	Rear panel	1	A8A5

Table 1-4. Equipment Required But Not Supplied

NAME	RECOMMENDED TYPE	MANUFACTURER	QTY
Headset-microphone	997-7419 Model 977	Electro-Voice, Inc.	1
Desk microphone	EV629-7929	Electro-Voice, Inc.	1
Telegraph key	CD-201A	Winslow Tele-Tronics, Inc.	1

CHAPTER 2

INSTALLATION

2-1. INTRODUCTION. This chapter furnishes all the information required to install the Control-Monitor Group OK-145/TSC-60(V) (radio control group). Section I of this chapter contains the data required for installation planning; section II contains a tabulation of the equipment shipped and provides complete logistical data; and section III provides the step-by-step installation instructions. Equipment reshipment information is presented in section IV.

SECTION I

INSTALLATION PLANNING

2-2. EQUIPMENT LOCATION.

2-3. The radio control group is designed for use in a standard 19-inch equipment rack and requires 7 inches of panel height. The primary installation requirements are that the equipment rack be at least 12 inches deep to accommodate the 11-inch panel and the required cable connectors that must be mounted on the rear. When properly insulated and shielded cables are provided, the radio control group can be located as far as 1/4 mile from the associated radio equipment.

2-4. WIRING REQUIREMENTS.

2-5. The power and signal connectors on the rear of the radio control group must be connected to the associated radio equipment and the required 120-volt ac power source to complete the continuity of the communications system in which the radio control group is operated.

SECTION II

LOGISTICS

2-6. RECEIVING DATA.

2-7. Table 2-1 lists the equipment shipped and includes the following data: uncrated dimensions and crated dimensions (estimated); volume (estimated); and gross weight (estimated). Preservation, packaging, and packing shall be in accordance with section 5 (Preparation for Delivery) of MIL-S-52059B (EL) Amendment 1, dated 20 December 1963.

2-8. TRANSPORTABILITY.

2-9. A crated radio control group can be transported to any site by any vehicle that may be available and appropriate.

2-10. RECEIPT AND UNPACKING.

2-11. The radio control group is assembled and ready for use prior to shipment from the factory, except for interconnecting and power cabling. When uncrating the equipment, use extreme care to prevent damage to the unit and the packing materials (crates and insulation) that may be needed for repacking and reshipment of the equipment at a future date. Each unit of the equipment should be thoroughly inspected for physical damage when it is unpacked. If damage is found, notify the appropriate authority so a claim can be initiated with the carrier.

Table 2-1. Radio Control Group Crated and Uncrated Dimensions and Weights

CRATED (approx)			UNCRATED	
DIMENSIONS (inches)	VOLUME (cu ft)	WEIGHT (lb)	DIMENSIONS (inches)	WEIGHT (lb)
Height 10	1.58	47	Height 7	42
Width 21			Width 19	
Depth 13			Depth 11	

2-12. CABLE REQUIREMENTS.

2-13. The proper type and size of wire to be used to connect the radio control group to the radio equipment and the power source is shown in the installation wiring diagrams and/or wiring tables of the particular system in which the radio control group is used.

SECTION III

INSTALLATION PROCEDURES

2-14. RACK MOUNTING AND CABLE INSTALLATION.

2-15. Install the radio control group in the appropriate equipment rack using standard-practice installation procedures. Use the applicable system wiring diagram and/or wiring tables to determine the proper signal and power cables that must be connected to the connectors on the rear of the radio control group. It is necessary to move the radio control group forward out of the equipment rack while the cable connections are being made. After the cable connections are made, secure the radio control group in the equipment rack. No special installation tools or materials are required to complete the installation. For more detailed information concerning location and cable hookup, refer to the equipment group manuals listed in chapter 5 of this manual.

2-16. POST-INSTALLATION TEST.

2-17. Upon completion of the installation, a complete performance test of the radio control group is required to ensure that the installation has been completed satisfactorily. Refer to chapter 5 of this manual for information on testing procedures and performance standards.

SECTION IV

PREPARATION FOR RESHIPMENT

2-18. DISASSEMBLY.

2-19. Ensure that primary power is removed from the radio control group. Remove the radio control group from the equipment rack and disconnect the power and signal cables by reversing the procedure presented in paragraph 2-14.

2-20. REPACKAGING INSTRUCTIONS.

2-21. No special instructions are required to package the radio control group for reshipment. Repack the equipment in the original packing case (if available) using sufficient insulation to provide adequate cushioning between the equipment and the case. Dessicant dehydrators (Military Specification MIL-D-9394 or equivalent) should be included in the shipping case.

2-22. If it should become necessary to ship the audio control unit or either the transmit or receive control head separately, fabricate an appropriate case using the same general procedure described for shipping the complete equipment.

CHAPTER 3

OPERATION

3-1. INTRODUCTION. This chapter contains operating instructions for the Control-Monitor Group OK-145/TSC-60(V) (radio control group). Section I describes the controls and indicators used to control and operate associated radio equipment. Section II describes the turn-on, operation, and turn-off procedures. Section III, Emergency Operation, is not applicable.

SECTION I

CONTROLS AND INDICATORS

3-2. Tables 3-1 through 3-3 list and describe the controls and indicators of Transmitter Control C-8363/TSC-60(V) (transmit control head), Receiver Control C-8362/TSC-60(V) (receive control head), and Control-Monitor C-8364/TSC-60(V) (audio control unit). All the operational controls and indicators are on the equipment front panel and are shown in figure 3-1.

Table 3-1. Transmit Control Head, Controls and Indicators

NAME	REFERENCE DESIGNATION	FUNCTION
XMIT PWR switch	A7A9S1	Controls switched dc voltages to the radio transmitter.
OFF		Disables all the radio transmitter switched dc voltages except the continuous DCU/DCFE power.
STBY		Selects standby (filament on) operation of the radio transmitter.
HIGH		Selects high-power operation of the radio transmitter and enables plate voltage.
LOW		Selects low-power operation of the radio transmitter and enables plate voltage.
KEY-OFF-VOX/PTT switch	A7A9S2	Enables radio transmitter key options through controls of audio control unit.
KEY		Permits the computer to key the transmitter if XMIT PWR switch A7A9S1 is in either the HIGH or LOW position.

Table 3-1. Transmit Control Head, Controls and Indicators (Cont)

NAME	REFERENCE DESIGNATION	FUNCTION
OFF		Disables computer control of the radio transmitter key line during normal operation.
VOX/PTT		Permits external keying of the radio transmitter by detectors in the exciter, a push-to-talk microphone, or a cw key depending upon the position of XMIT PWR switch A7A9S1, SELF TEST/AM/CW switch A7A9S7, and VOX-CW/PTT switch S8 (on the audio control unit).
CARR LEVEL selector switch	A7A9S3	Selects the carrier level of the radio transmitter.
OFF		Selects maximum carrier suppression (approximately -60 dB below the pep).
-30 to 0		Selects carrier level suppression from -30 to 0 dB (maximum carrier transmitted) in steps of 3 dB.
LAMP TEST pushbutton switch	A7A9S4	When pressed and held in position, lights the FAULT, UNIT PWR, OPR, PROVE, KEYED, and INITIATE indicators to the level of brilliance determined by LAMP DIM control A7A9R1. When the LAMP TEST pushbutton is released, the indicators return to the display status previous to the lamp test or to an updated status.
MODE A2 selector switch	A7A9S5	Controls the operational mode of transmitter sideband A2.
OFF		Disables transmitter sideband A2.
ON		Enables transmitter sideband A2 providing SELF TEST/AM/CW switch A7A9S7 is in the independent-sideband (unlabeled left) position or the SELF TEST position.
MODE B2 selector switch	A7A9S6	Controls the operational mode of transmitter sideband B2.
OFF		Disables transmitter sideband B2.

Table 3-1. Transmit Control Head, Controls and Indicators (Cont)

NAME	REFERENCE DESIGNATION	FUNCTION
ON		Enables transmitter sideband B2 providing SELF TEST/AM/CW switch A7A9S7 is in the independent-sideband (unlabeled left) position or the SELF TEST position.
SELF TEST/AM/CW selector switch	A7A9S7	Selects the operating modes of the radio transmitter.
Independent-sideband position (unlabeled left position)		Enables control of MODE A1, A2, B1, and B2 selector switches.
SELF TEST		Enables control of MODE A1, A2, B1, and B2 selector switches and the transmitter self-test routine. The self test is verified when PROVE indicator A7A9DS4 lights indicating that the radio transmitter is operating properly in the modes selected.
AM		Disables MODE A1, A2, B1, and B2 selector switches and enables the radio transmitter for amplitude modulation equivalent (AME) operation.
CW A1		Disables control of MODE A1, A2, B1, and B2 selector switches and enables the radio transmitter for cw operation on sideband A1.
CW B1		Disables control of MODE A1, A2, B1, and B2 selector switches and enables the radio transmitter for cw operation on sideband B1.
MODE A1 selector switch	A7A9S8	Controls operational mode of transmitter sideband A1.
OFF		Disables transmitter sideband A1.
ON		Enables transmitter sideband A1.
MODE B1 selector switch	A7A9S9	Controls operational mode of transmitter sideband B1.
OFF		Disables transmitter sideband B1.
ON		Enables transmitter sideband B1.

Table 3-1. Transmit Control Head, Controls and Indicators (Cont)

NAME	REFERENCE DESIGNATION	FUNCTION
FREQUENCY-MHZ thumbwheel switch	A7A9S10	Controls the operating frequency of the radio transmitter. Positioning the six decade thumbwheels selects operating frequencies from 2 to 29.9999 MHz in increments of 0.1 kHz. When any one of the decade thumbwheels is repositioned, INITIATE indicator A7A9DS6 lights.
INITIATE indicator push-button switch	A7A9S11	When pressed momentarily, enables the computer to transmit the radio transmitter frequency data set by FREQUENCY-MHZ thumbwheel switch A7A9S10 and also transmits mode data.
FAULT indicator (red)	A7A9DS1	When lighted, indicates a fault in the transmitter tune cycle, a power fault, or a fault in the CCCS link that connects the radio control to the transmitter. Once lighted, the indicator remains lighted until the fault is corrected. In the event of a CCCS link fault, the indicator remains lighted until the INITIATE switch is depressed.
UNIT PWR indicator (green)	A7A9DS2	When lighted, indicates that transmit control head power supply A7A10PS1 is supplying power to the internal logic circuits.
OPR indicator (green)	A7A9DS3	When lighted, indicates that the radio transmitter is ready to transmit (tuned, plate voltage enabled).
PROVE indicator (green)	A7A9DS4	Indicator lights when the transmitter is placed in the self-test mode and the equipment successfully completes the self-test routine. The indicator is off when the self-test mode is not selected or when the equipment fails to complete the self-test routine.
KEYED indicator (green)	A7A9DS5	When lighted, indicates the power amplifier has received a key command.

Table 3-1. Transmit Control Head, Controls and Indicators (Cont)

NAME	REFERENCE DESIGNATION	FUNCTION
INITIATE indicator (blue)	A7A9DS6	When lighted, indicates that the frequency or mode data should be reinitiated by pressing INITIATE pushbutton switch A7A9S11. The indicator lights when any of the FREQUENCY-MHZ thumbwheels are repositioned, if there is a power interruption, if there is a DCU address error, if there is a power or tune fault, or if the XMIT PWR switch is repositioned.
LAMP DIM control	A7A9R1	Controls the brilliance (illumination) of FAULT, UNIT PWR, OPR, PROVE KEYED, and INITIATE indicators. Clockwise rotation increases the brilliance and counterclockwise rotation reduces the brilliance.

Table 3-2. Receive Control Head, Controls and Indicators

NAME	REFERENCE DESIGNATION	FUNCTION
LAMP DIM control	A8A4R1	Controls the brilliance (illumination) of INITIATE, PROVE, OPR, FAULT, and UNIT PWR indicators. Clockwise rotation increases the brilliance and counterclockwise rotation reduces the brilliance.
RCVR PWR OFF/ON switch	A8A4S1	
OFF		Disables all the radio receiver power supply voltages except the DCU/DCFE voltages.
ON		Enables all the radio receiver power supply voltages except the DCU/DCFE voltages.
SQUELCH B selector switch	A8A4S2	Varies the sensitivity of receiver squelch for sidebands B1 and B2.
OFF		Removes all squelch control from receiver sidebands B1 and B2.

Table 3-2. Receive Control Head, Controls and Indicators (Cont)

NAME	REFERENCE DESIGNATION	FUNCTION
Positions 1 through 9		Varies the sensitivity of receiver squelch for sidebands B1 and B2. Position 1 represents minimum squelch and position 9 represents maximum squelch.
SQUELCH A selector switch	A8A4S3	Varies the sensitivity of receiver squelch for sidebands A1 and A2.
OFF		Removes all squelch control from receiver sidebands A1 and A2.
Positions 1 through 9		Varies sensitivity of receiver squelch for sidebands A1 and A2. Position 1 represents minimum squelch and position 9 represents maximum squelch.
LAMP TEST pushbutton switch	A8A4S4	When pressed and held in position, lights the FAULT, UNIT PWR, OPR, PROVE, and INITIATE indicators to the level of brilliance determined by LAMP DIM control A8A4R1. When the LAMP TEST pushbutton is released, the indicators return to the display status previous to the lamp test or to an updated status.
MODE A2 selector switch	A8A4S5	Controls the operational mode and agc action of receiver sideband A2.
OFF		Disables reception of receiver sideband A2.
VOICE		Enables agc action appropriate for voice reception on receiver sideband A2.
DATA 1		Enables agc action appropriate for tactical digital information link (TADIL) A reception on receiver sideband A2.
DATA 2		Enables agc action appropriate for reception of fsk tty and tactical digital information link (TADIL) B on receiver sideband A2.
MODE B2 selector switch	A8A4S6	Controls the operational mode and agc action of receiver sideband B2.
OFF		Disables reception of receiver sideband B2.

Table 3-2. Receive Control Head, Controls and Indicators (Cont)

NAME	REFERENCE DESIGNATION	FUNCTION
VOICE		Enables agc action appropriate for voice reception on receiver sideband B2.
DATA 1		Enables agc action appropriate for TADIL A reception on receiver sideband B2.
DATA 2		Enables agc action appropriate for reception of fsk tty and TADIL B on receiver sideband B2.
SELF TEST/AM/SELF TEST selector switch	A8A4S7	Selects the operating modes of the radio receiver.
Independent-sideband position (unlabeled left)		Enables control of MODE A1, A2, B1, and B2 selector switches.
Independent-sideband SELF TEST		Enables control of MODE A1, A2, B1, and B2 selector switches and enables self-test routine for the operationals modes selected by the switches. Successful completion of the self test is verified when PROVE indicator A8A4DS4 lights, indicating that audio is being received on the selected channels, all agc circuits are functioning properly, and no other faults exist.
AM		Disables MODE A1, A2, B1, and B2 selector switches and permits reception of amplitude modulated (AM) signals by the radio receiver.
AM SELF TEST		Disables MODE A1, A2, B1, and B2 selector switches and permits self testing of the radio receiver am operation. This self test is verified when PROVE indicator A8A4DS4 lights, indicating that the required am audio signal is being received, all agc circuits are functioning properly, and no other faults exist.
MODE A1 selector switch	A8A4S8	Controls the operational and agc action mode of receiver sideband A1.
OFF		Disables reception of receiver sideband A1.

Table 3-2. Receive Control Head, Controls and Indicators (Cont)

NAME	REFERENCE DESIGNATION	FUNCTION
VOICE		Enables agc action appropriate for voice reception on receiver sideband A1.
DATA 1		Enables agc action appropriate for TADIL A reception on receiver sideband A1.
DATA 2		Enables agc action appropriate for reception of fsk tty and TADIL B on receiver sideband A1.
MODE B1 selector switch	A8A4S9	Controls the operational mode and agc action of receiver sideband B1.
OFF		Disables reception of receiver sideband B1.
VOICE		Enables agc action appropriate for voice reception on receiver sideband B1.
DATA 1		Enables agc action appropriate for TADIL A reception on receiver sideband B1.
DATA 2		Enables agc action appropriate for reception of fsk tty and TADIL B on receiver sideband B1.
FREQUENCY-MHZ thumbwheel switch	A8A4S10	Controls the operating frequency of the radio receiver. Positioning the six decade thumbwheels selects operating frequencies from 2 to 29.9999 MHz in increments of 0.1 kHz. When any one of the decade thumbwheels is repositioned, INITIATE indicator A8A4DS5 lights.
INITIATE indicator push-button switch	A8A4S11	When pressed momentarily, enables the transmission of receiver mode and frequency data set by FREQUENCY-MHZ thumbwheel switch A8A4S10 and other front panel controls.

Table 3-2. Receive Control Head, Controls and Indicators (Cont)

NAME	REFERENCE DESIGNATION	FUNCTION
INITIATE indicator (blue)	A8A4DS5	When lighted, indicates that one or more of the FREQUENCY-MHZ thumbwheels have been repositioned or that the receive control head has detected an internal power interruption, a tune fault, a power fault, an equipment power interrupt, or control link error. Once lighted, the indicator remains lighted until the INITIATE pushbutton switch is pressed to reset the indicator to off or until the fault is corrected.
PROVE indicator (green)	A8A4DS4	When lighted, indicates that SELF TEST/ AM/SELF TEST switch A8A4S7 is operating properly in either the independent-sideband SELF TEST or the AM/SELF TEST mode.
OPR indicator (green)	A8A4DS3	When lighted, indicates the radio receiver is tuned and ready for operation (tuned, no faults, and power on).
UNIT PWR indicator (green)	A8A4DS2	When lighted, indicates that receive control head power supply A8A5PS1 is supplying required power to the internal logic circuits.
FAULT indicator (red)	A8A4DS1	When lighted, indicates a fault condition within the receive control head or an internal power interruption, a tune fault, a power fault, a receiver overload fault, or a CCCS bus fault. Once lighted, the indicator remains lighted until the fault is corrected or until power has been restored to normal.

Table 3-3. Audio Control Unit, Controls and Indicators

NAME	REFERENCE DESIGNATION	FUNCTION
POWER ON/OFF circuit breaker	CB1	Provides overload protection for the 120-volt ac input power and serves as an on/off switch for the radio control group.
ON		Applies 120 volts ac to power supplies PS1, A7A10PS1, and A8A5PS1. Also applies 120 volts ac through a dimmer circuit to the front panel edge-lighting circuits of the transmit and receive control heads and the audio control unit.
OFF		Removes all power from the radio control group.
SIMPLEX/DUPLEX switch	S1	
SIMPLEX		Causes the computer to enable simplex operation of the radio equipment.
DUPLEX		Causes the computer to disable simplex operation of the radio equipment and thus enable the normal duplex operation.
A2 RCV MON/OFF/OPR switch	S2	
RCV MON		Enables the operator to monitor any audio signals present on independent-sideband channel A2. Received audio is routed through a high-impedance bridge to speaker LS1 or an external headset.
OFF		Disables operator reception of audio on independent-sideband channel A2.
OPR		Connects the amplified microphone output to the A2 transmit line and enables application of signals received on independent-sideband channel A2 through a 600-ohm termination to the speaker or the headset.
A1 RCV MON/OFF/OPR switch	S3	Provides the same functions as switch S2, except that it controls the audio lines for independent-sideband channel A1.
B1 RCV MON/OFF/OPR switch	S4	Provides the same functions as switch S2, except that it controls the audio lines for independent-sideband channel B1.

Table 3-3. Audio Control Unit, Controls and Indicators (Cont)

NAME	REFERENCE DESIGNATION	FUNCTION
B2 RCV MON/OFF/OPR switch	S5	Provides the same functions as switch S2, except that it controls the audio lines for independent-sideband channel B2.
ORDER WIRE LISTEN/OFF/ TALK switch	S6	Controls operation of order-wire circuit.
LISTEN		A locking position that enables the operator to monitor audio transmitted over the order wire.
OFF		A locking position that disables the transmit and receive functions of the order wire at the associated audio control unit.
TALK		A momentary position that enables the operator to transmit on the order-wire circuit.
SPKR/HDST switch	S7	
SPKR		Applies selected audio to speaker LS1 on the audio control panel.
HDST		Applies selected audio to an external headset through jack J3 on the front of the audio control unit.
VOX-CW/PTT switch	S8	
VOX		Causes the computer to enable the VOX keying circuits of the radio equipment. (This switch is electrically interlocked with the XMIT PWR, KEY-OFF-VOX/ PTT, and the SELF TEST/AM/CW switches on the transmit control head and disables cw/ptt operation from the audio control unit.)
CW/PTT		Causes the computer to disable the VOX keying circuits of the radio equipment and enables the cw and ptt key circuits.
POWER indicator (green)	DS1	When lighted, indicates that the receive control head power supply A8A5PS1 is supplying power to the indicator lamps on the audio control unit.

Table 3-3. Audio Control Unit, Controls and Indicators (Cont)

NAME	REFERENCE DESIGNATION	FUNCTION
A2 indicator (white)	DS2	When lighted, indicates audio is present on independent-sideband channel A2.
A1 indicator (white)	DS3	When lighted, indicates audio is present on independent-sideband channel A1.
B1 indicator (white)	DS4	When lighted, indicates audio is present on independent-sideband channel B1.
B2 indicator (white)	DS5	When lighted, indicates audio is present on independent-sideband channel B2.
VOL control	R41	Controls the level of the audio applied to speaker LS1 or the external headset.
DIM control	R42	Controls the brilliance of the front panel edge-lighting on the transmit and receive control heads and the audio control unit.
Microphone/headset jack	J3	Provides connection for an external push-to-talk desk microphone or headset microphone.
CW KEY jack	J4	Provides connection for an external cw key.
Audio control unit speaker	LS1	Monitors audio selected by front panel controls.

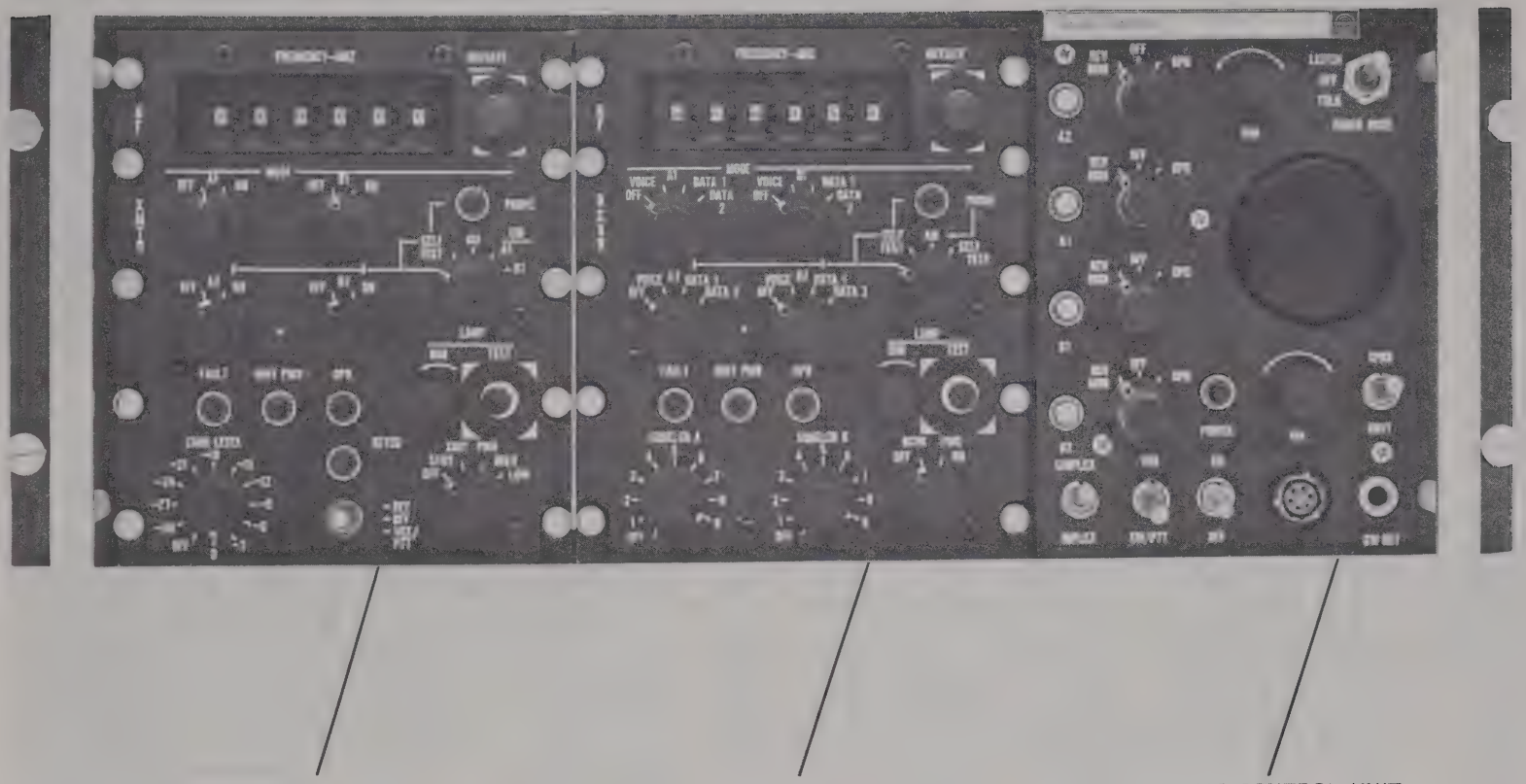


Figure 3-1. Radio Control Group, Controls and Indicators

SECTION II

OPERATING INSTRUCTIONS

3-3. GENERAL.

3-4. This section contains the turn-on, operating, and turn-off procedures for the radio control group. Because the equipment is a control panel for an associated radio set, the following procedures assume the compatible radio equipment is properly connected and is functioning satisfactorily. Refer to tables 3-1 through 3-3 for control and indicator information.

3-5. TURN-ON PROCEDURE.

3-6. To turn on the radio control group, proceed as follows:

a. Set POWER ON-OFF circuit breaker CB1 on the audio control panel to ON.

b. Rotate LAMP DIM controls A7A9R1 and A8A4R1 on the transmit and receive control heads fully clockwise.

c. Observe that the following indicators light.

Power indicator DS1 on the audio control unit.

UNIT PWR indicator A7A9DS2, FAULT indicator A7A9DS1, and INITIATE indicator A7A9DS6 on the transmit control head.

Indicator lamps of FREQUENCY-MHZ switches A7A9S10 and A8A4S10 on the transmit and receive control heads.

UNIT PWR indicator A8A4DS2, FAULT indicator A8A4DS1, and INITIATE indicator A8A4DS5 on the receive control head.

d. Rotate DIM control R42 on the audio control panel fully clockwise and observe that the edge lighting (labeling) on the audio control unit, the transmit control head, and the receive control head lights.

e. Rotate the DIM control counter clockwise and observe that the brilliance of the edge lighting on the three front panels varies accordingly. Set the brilliance to the desired level.

f. Momentarily press LAMP TEST pushbutton switch A7A9S4 on the transmit control head and observe that all the indicators on the transmit control head light.

g. Momentarily press LAMP TEST pushbutton switch A8A4S4 on the receive control head and observe that all the indicators on the receive control head and the audio control unit light.

3-7. OPERATING PROCEDURE.

3-8. TRANSMITTER OPERATION. The transmitting equipment controlled by the transmit control head operates on independent sideband channels A1, A2, B1, and B2 or any combination of these channels selected by the front panel switches. Operation of these four voice channels simultaneously transmits tty, voice, or tactical digital information in the normal operational configuration. During this type operation, the transmitter carrier level is normally suppressed by setting CARR LEVEL switch A7A9S3 to OFF. This switch is operative at all times and the transmit control head sends the carrier level information to the transmitter whether it is used or not. The switch also varies the suppression of the transmitter carrier from -30 to 0 dB (referenced to maximum carrier transmitted). Varying the suppression in this manner provides the amount of carrier needed by the radio receiver receiving the high-frequency transmissions. To set up the radio transmitter for normal operation on the four independent-sideband channels, refer to the applicable radio equipment technical manuals and perform any preliminary operations that are required. At the radio control group, set the front panel controls and observe the indications listed below.

a. Set POWER ON/OFF circuit breaker CB1 on the audio control unit to OFF.

b. Set switches on the transmit control head as follows:

XMIT PWR switch A7A9S1 to OFF

CARR LEVEL switch A7A9S3 to OFF

Independent-sideband switches A2 (A7A9S5), B2 (A7A9S6), A1 (A7A9S8), and B1 (A7A9S9) to OFF

KEY-OFF-VOX/PTT switch A7A9S2 to OFF

SELF TEST/AM/CW selector switch A7A9S7 to the independent-sideband position (unlabeled left position)

c. Perform the turn-on procedures listed in paragraph 3-5.

d. Rotate the six thumbwheels of FREQUENCY-MHZ switch A7A9S10 on the transmit control head until the desired transmitter frequency is visible in the lighted thumbwheel indicators.

e. Set XMIT PWR switch A7A9S1 to STBY and momentarily press INITIATE pushbutton switch A7A9S11. Observe that KEYED indicator A7A9DS5 flashes momentarily, FAULT indicator A7A9DS1 stays on, INITIATE indicator A7A9DS6 goes out, and OPR indicator A7A9DS3 remains off. Allow sufficient time for the transmitter to warm up. The 1-kW transmitter usually requires approximately 5 minutes and the 2.5- and 10-kW transmitters require approximately 30 seconds. Set XMIT PWR switch A7A9S1 to HIGH and momentarily press INITIATE pushbutton switch A7A9S11. INITIATE indicator A7A9DS6 goes out. Set KEY-OFF-VOX/PTT switch A7A9S2 to KEY and then to OFF. This key command enables the transmitter to tune. Observe that KEYED indicator A7A9DS5 lights. When the transmitter is tuned, the KEYED and FAULT indicators go out and the OPR indicator lights.

f. Set independent-sideband switches A1, A2, B1, and B2 (A7A9S5, S6, S8, and S9) to ON or OFF depending upon the channels required for the particular operation.

g. Set SELF TEST/AM/CW switch A7A9S7 to SELF TEST and KEY-OFF-VOX/PTT switch A7A9S2 to KEY. Observe that PROVE indicator A7A9DS4, KEYED indicator A7A9DS5, and OPR indicator A7A9DS3 light.

NOTE

A lighted PROVE indicator indicates that the computer has successfully completed a self-test routine of the transmitter equipments.

h. Set KEY-OFF-VOX/PTT switch A7A9S2 to OFF and observe that the KEYED indicator goes out, and the PROVE indicator remains on.

i. Set the SELF TEST/AM/CW switch to the independent-sideband (unlabeled left) position. Observe that the PROVE indicator goes out and the OPR indicator remains lighted.

j. Set the KEY-OFF-VOX/PTT switch to the type of transmitter keying required. If tty data is to be transmitted, the switch should be set to KEY. If only single-channel voice is to be transmitted, the switch should be set to VOX/PTT. In this instance VOX-CW/PTT switch S8 on the audio control unit should be set to VOX if the vox units of the radio equipment are used to key the transmitter or to CW/PTT if an external microphone key or cw key is used to key the transmitter.

3-9. To operate the radio transmitter in the am mode, follow the procedure listed in steps a. through e. of paragraph 3-8 and continue as follows.

a. Set SELF TEST/AM/CW switch A7A9S7 to AM. In this position the four independent-sideband switches (A1, A2, B1, and B2) are disabled, and the radio transmitter is set up for amplitude modulation of the upper-sideband carrier.

b. Set KEY-OFF-VOX/PTT switch A7A9S2 to VOX/PTT or KEY.

c. Set VOX-CW/PTT switch S8 on the audio control panel to either position, depending upon the type of keying desired.

3-10. To operate the radio transmitter in the cw mode, follow the procedure listed in steps a. through e. of paragraph 3-8 and continue as follows.

a. Set SELF TEST/AM/CW switch A7A9S7 to CW A1 or CW B1. In either of these positions the four independent-sideband switches (A1, A2, B1, and B2) are disabled and the radio transmitter is

set up for cw operation on independent-sideband channel A1 or B1 depending upon the position of switch A7A9S7.

b. Set KEY-OFF-VOX/PTT switch A7A9S2 to VOX/PTT.

c. Set VOX-CW/PTT switch A8 on the audio control unit to CW/PTT.

3-11. RECEIVER OPERATION. The receiving equipment controlled by the receive control head also operates on independent-sideband channels A1, A2, B1, and B2 or any combinations of these channels selected by the front panel switches. The type of reception on each of these channels is also selected by the individual switches. Each switch selects compatible agc action for either voice, tty, or tactical digital information reception or turns the channel off. To set up the receiver for normal operation on the four independent-sideband channels, refer to the applicable radio equipment technical orders and perform any preliminary operations that are required. At the radio control group set the front panel controls and observe the instructions listed below.

a. Set POWER ON/OFF circuit breaker CB1 on the audio control unit to OFF.

b. Set switches on the receive control head as follows:

RCVR PWR OFF/ON switch A8A4S1 to OFF.

SQUELCH B and SQUELCH A switches A8A4S2 and S3 to OFF.

Independent-sideband switches A2 (A8A4S5), B2 (A8A4S6), A1 (A8A4S8), and B1 (A8A4S9) to OFF.

SELF TEST/AM/SELF TEST switch to the independent-sideband (unlabeled left) position.

c. Perform the turn-on procedure given in paragraph 3-5.

d. Rotate the six thumbwheels of FREQUENCY-MHZ switch A8A4S10 on the receive control head until the desired receiver frequency is visible in the lighted thumbwheel indicators.

e. Set RCVR PWR switch A8A4S1 to ON. Observe that FAULT indicator A8A4DS1 and INITIATE indicator A8A4DS5 are on and OPR indicator A8A4DS3 is out.

f. Momentarily press INITIATE pushbutton switch A8A4S11. Allow approximately 10 seconds for the receiver to change frequency and tune; then, observe that the FAULT indicator goes out and the OPR indicator lights. The INITIATE indicator goes out when switch A8A4S1 is pressed.

g. Set SPKR/HDST switch S7 on the audio control unit to SPKR.

h. On the audio control unit set RCV MON/OFF/OPR switches (S2 through S5) for channels A2, A1, B1, and B2 to OPR.

NOTE

During the following steps, noise is heard from the speaker on the audio control unit when such noise is present on a channel. In the receiver SELF TEST mode, broadband noise is injected into the receiver. Therefore, a high level of random noise is heard over the speaker. Set VOL control R41 on the audio control unit for a comfortable listening level.

i. Set SELF TEST/AM/SELF TEST switch A8A4S7 to independent-sideband SELF TEST (second position from left).

j. Switch independent-sideband A2 (A8A4S5) sequentially to VOICE, DATA 1, DATA 2, and OFF. Observe that PROVE indicator A8A4DS4 lights at each switch position including OFF, A2 channel indicator DS2 on the audio control unit lights, and noise is heard from the speaker on the audio control unit in each position except OFF.

k. Repeat step j. sequentially using controls for channels A1, B1, and B2. Observe the same indications on PROVE indicator A8A4DS4 and channel indicators A1, B1, and B2 (DS3, DS4, and DS5) on the audio control unit when the associated channels are enabled.

l. Set SELF TEST/AM/SELF TEST to AM SELF TEST (extreme right position). Observe that PROVE indicator A8A4DS4 and channel indicator A1 (DS3) light and noise is heard from the speaker.

m. Set SELF TEST/AM/SELF TEST switch A8A4S7 to the independent-sideband (unlabeled left) position. If AM operation is desired, set switch to AM.

n. Set the four independent-sideband switches for channels A1, A2, B1, and B2 to the desired setting to accommodate the type of reception required.

3-12. TURN-OFF PROCEDURE.

3-13. To turn off the radio control group and the transmitting and receiving equipment it controls, proceed as follows.

a. Set XMIT PWR switch A7A9S1 to OFF and observe that the OPR indicator goes out. If the transmitter is shut off for a short period, it may be desirable to set the switch to STBY and have the transmitter in a filament on condition. In these instances, do not remove primary power from the radio control group.

b. Set RCVR PWR switch A8A4S1 to OFF and observe that OPR indicator goes out.

c. Set POWER ON/OFF circuit breaker CB1 on the audio control unit to OFF.

SECTION III

EMERGENCY OPERATION

NOT APPLICABLE

CHAPTER 4

PRINCIPLES OF OPERATION

4-1. INTRODUCTION. The three sections of this chapter describe the principles of operation of the Control-Monitor Group OK-145/TSC-60(V) (radio control group). Section I describes the functions of the equipment on a signal flow basis. An overall functional block diagram supports the description. Section II describes the functional operation of electronic circuits. A combination of schematic and detailed logic diagrams are provided to support the descriptions. Section III, Functional Operation of Mechanical Assemblies, is not applicable. Refer to T.O. 31-1-141, Basic Electronics Technology and Testing Practices, for basic circuit principles of operation.

SECTION I

FUNCTIONAL SYSTEM OPERATION

4-2. GENERAL.

4-3. The radio control group provides complete control, monitoring, and operating facilities for an hf receiver and transmitter set that includes a power amplifier, an exciter, an antenna coupler, and a maintenance display. The transmitter and receiver functions are separate and are controlled by Transmitter Control C-8363/TSC-60(V) (transmit control head) and Receiver Control C-8362/TSC-60(V) (receive control head) that are electrically and mechanically interfaced with Control-Monitor C-8364/TSC-60(V) (audio control unit). However, the receive and transmit control heads share the read only memory (rom) computer that is part of the transmit control head. The basic functions of the transmit and receive control heads and the audio control unit are summarized in the following paragraphs.

4-4. TRANSMIT CONTROL HEAD. The transmit control head provides a selection of 280,000 communications channels covering the frequency range from 2.0000 to 29.9999 MHz in 100-Hz increments. Frequency selection is implemented by manually positioning six direct-reading, decade rotary thumbwheel switches. The associated transmitter is automatically tuned to the selected frequency when the INITIATE pushbutton on the transmit control head is pressed.

4-5. Four switches select the on/off operation of the transmitter independent-sideband channels. These sideband channels are designated; upper sideband (usb) A1, upper upper sideband (uusb) A2, lower sideband (lsb) B1, and lower lower sideband (llsb) B2. The independent sideband switches are electrically interlocked with a mode selector switch that causes the rom computer to initiate a self-test routine on the selected sideband channels or disables the independent sideband switches and selects either amplitude modulation equivalent (AME) operation or cw operation on sideband channels A1 or B1. The mode selector switch is also electrically interlocked with the transmitter power control switch and the key line selector switch. This interlock arrangement ensures that the transmitter is operating on high or low power (plate voltage enabled) before the transmitter can be keyed by the front panel key switch. A carrier level switch provides variable suppression of the transmitter carrier over a range of 0 (maximum carrier transmitter to approximately -60 dB below the pep (maximum carrier suppression). Suppression is selectable in 3-dB increments. Front panel indicator lamps reflect the operational status of the transmitter that is continuously updated by the rom computer.

4-6. RECEIVE CONTROL HEAD. The receive control head provides the same frequency selection for the receiver as that described for the transmit control head in paragraph 4-4. This control head also has four independent-sideband channel selector switches. Each of these switches enables the channel and selects agc action appropriate for either voice operation, teletypewriter

operation, TADIL operation, or turns the respective sideband channel off. The independent-sideband channel switches are electrically interlocked with a mode selector switch that causes the rom computer to initiate a self-test routine on the selected sideband channels or disables the independent-sideband switches and selects an AME operation. A fourth position of the mode switch initiates an AME self-test routine to determine whether the required AME signal is received. Two squelch switches vary the squelch of receiver-sideband channels. Front panel indicators reflect the operational status of the receiver that is continuously updated by the rom computer.

4-7. AUDIO CONTROL UNIT. The audio control unit provides the mechanical and electrical interface for the transmit and receive control heads, amplification for the transmit and receive audio channels, an order wire, a monitor bus, and facilities for operating the associated radio set. Internal wiring of the unit supplies a logic level interface between the receive control head and the rom computer of the transmit control head. The only direct input to the rom computer from the audio control unit is through the SIMPLEX/DUPLEX and the VOX-CW/PTT switches on the front panel. These switches enable or disable logic circuits and cause the rom computer to select simplex or duplex operation and the type of keying used by the transmitter. A front panel-mounted speaker and a microphone/headset jack operate in conjunction with a selector switch that allows reception of all audio channels from either device. Headset and speaker level is controlled by a continuously adjustable volume control. Separate audio control switches provide independent control of the 600-ohm transmit/receive channels. These switches select a bridging receiver monitor, terminated (600 ohms) operate, or off position for each of the four audio channels. Individual indicators light when audio signals are present on the receiver audio channels. An order-wire facility, interfaced with the audio end devices, is controlled by a 3-position toggle switch on the front panel. Other controls of the unit include a power on/off switch and an associated indicator, a potentiometer that adjusts the brilliance of the front panel edge lighting of the entire radio control group, and a lamp test switch to test the indicator lamps of the audio control unit.

4-8. BLOCK DIAGRAM ANALYSIS.

4-9. The functional relationship of the radio control group subassemblies is illustrated in figure 4-1. In the following paragraphs, an overall functional description is presented on a signal flow basis.

4-10. ROM COMPUTER. A read only memory computer (rom) is the nucleus of the entire radio control group. This computer is part of the transmit control head and consists of hardwire memory card A7A2, CCCS timing card A7A3, processor card A7A4, instruction decode card A7A5, and accessible memory card A7A6. The computer contains a unique hardwire program that controls and monitors a complete radio set and a maintenance display unit. Two basic functions of the computer are supervision of 2-way data transfer between the transmit and receive control heads, the radio equipment, and the maintenance display; and direction of the logical analysis and modification of data required to control and monitor the radio set. This analysis and modification includes the following:

a. Determination of the status of the radio under control and the resultant modifications to control data required for transmitter tune control, and for sequencing equipment self-test routines.

b. Determination of the transfer link status and alterations to the control routine resulting from detected link faults.

c. Determination of radio set configuration (does the radio set include a receiver and a transmitter, what type of transmitter, does the transmitter include a coupler) and alterations to the control routine that ensure only those radio components present within the system are addressed by the computer.

4-11. Communication between the computer and the transmit and receive control heads is via a logic level bus and communication between the computer and the radio equipment is via the CCCS bus. To follow the signal flow presented in figure 4-1, an understanding of the composition and relationship of these two buses is essential.

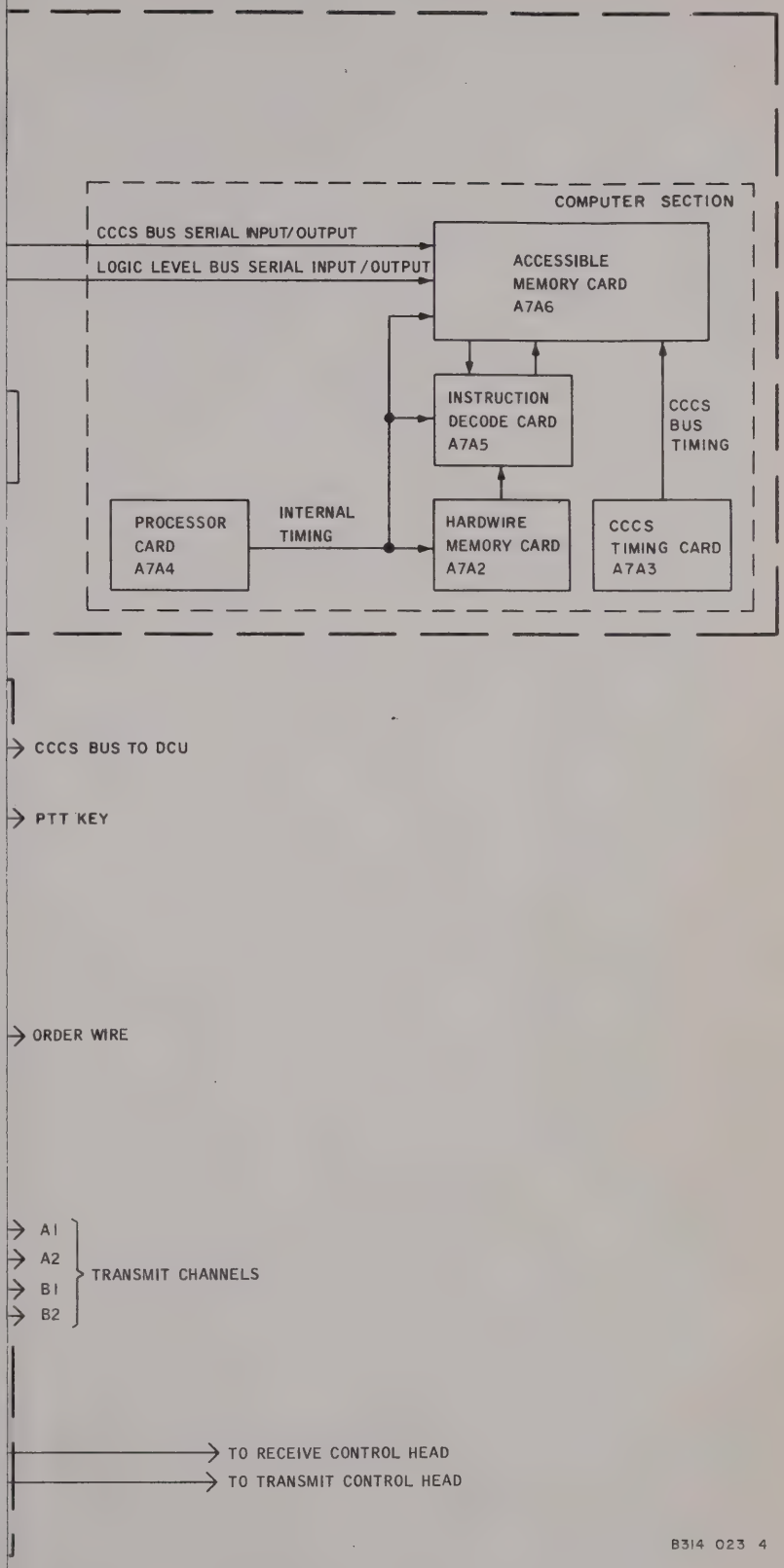


Figure 4-1. Radio Control Group, Functional Block Diagram

operation, TADIL operation, or turns the respective sideband channel off. The independent-sideband channel switches are electrically interlocked with a mode selector switch that causes the rom computer to initiate a self-test routine on the selected sideband channels or disables the independent-sideband switches and selects an AME operation. A fourth position of the mode switch initiates an AME self-test routine to determine whether the required AME signal is received. Two squelch switches vary the squelch of receiver-sideband channels. Front panel indicators reflect the operational status of the receiver that is continuously updated by the rom computer.

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c. Determination of radio set configuration (does the radio set include a receiver and a transmitter, what type of transmitter, does the transmitter include a coupler) and alterations to the control routine that ensure only those radio components present within the system are addressed by the computer.

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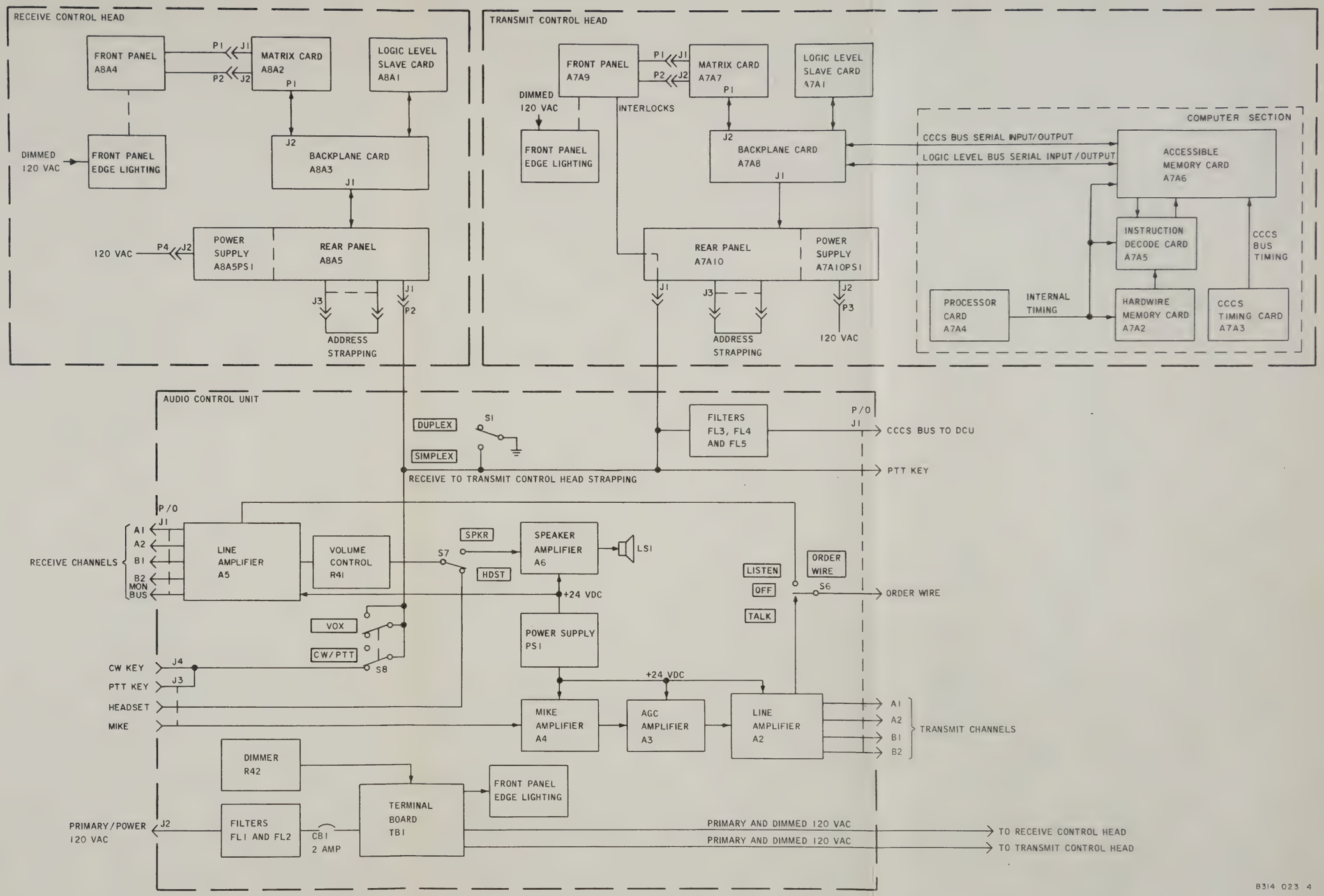


Figure 4-1. Radio Control Group, Functional Block Diagram

4-12. LOGIC LEVEL BUS. The logic level bus is the interface between the computer and the transmit and receive control heads. This bus consists of four pairs of wire commonly called the control bus, the monitor bus, the clock bus, and the delimiter bus. The data transferred via these buses is in serial word formats, the composition of which is described in subsequent paragraphs. Data is transmitted from the computer to the transmit and receive control heads by the control bus, and the monitor bus transfers data from the two control heads to the computer. The clock and delimiter buses are driven by computer processor card A7A4 and provide bit timing and word timing respectively. Figure 4-2 shows the relationship between the signals on the four buses that make up the logic level bus, and the following descriptions explain the functional character of these signals.

4-13. Clock Bus. The clock bus is a continuous square-wave signal symmetrical to within ±5 percent. This signal is used as an internal timing reference and is generated by processor card A7A4. A data transfer rate of 250 kilobits per second on the control and monitor buses is timed by the clock square-wave signal. The timing reference point is the falling edge of the clock signal.

4-14. Delimiter Bus. The signal on the delimiter bus is normally a logic 0, but is changed to a logic 1 during the 32-bit period that corresponds to the 32 bits of the control word (figure 4-2).

4-15. Control Bus. Data from the computer to the transmit and receive control heads consists of control words 32 bits long (numbered 0 through 31). The first seven bits (0 through 6) make up the address field. Bit 0 is not used and is transmitted as a logic 0. The functional equipment (receiver or transmitter) and data character (frequency, mode, monitor) address are contained in bits 1 through 4 and are a programmed function of the computer. Bits 5 and 6 identify the particular radio group being serviced. Selection is made by hardwire strapping at rear connectors on the transmit and receive control heads. The data field includes bits 7 through 31. However, bit 7 is used as the input/output bit and denotes the direction of data transfer (to or from the computer). This bit is always a logic 1 when the 24-bit control word data field

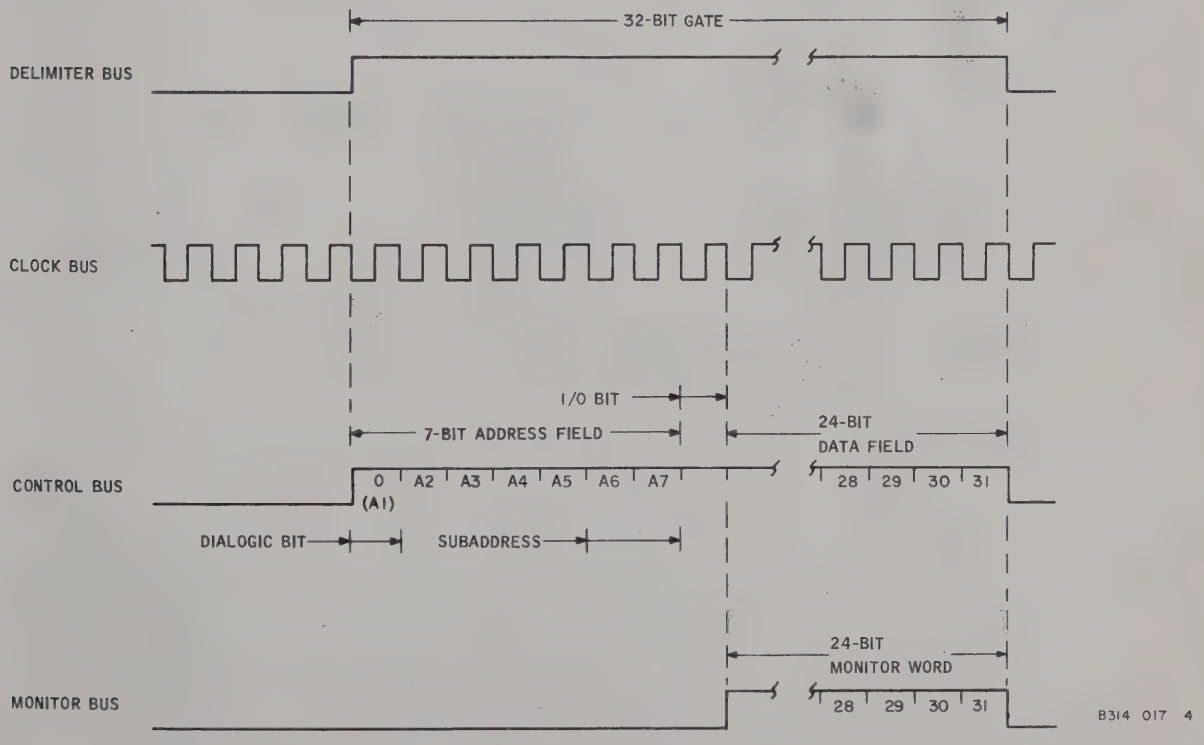


Figure 4-2. Logic Level Bus Signal Relationship

is examined and is a logic 0 if a monitor word is transmitted to the computer. When there is no data transferred on the control bus, a continuous logic 0 is present.

4-16. Monitor Bus. Data transferred from the transmit and receive control heads to the computer consists of three monitor words 24 bits long (numbered 0 through 23). The monitor words are transmitted from the respective control heads when the input/output bit (bit 7) of the control word is a logic 0. As shown in figure 4-2, timing of the monitor data is in-phase with the last 24 bits of the control word. The monitor bus is an open circuit when no data is being transferred.

4-17. Logic Level Monitor Word Formats. Three monitor words are transmitted on the logic level bus between each of the control heads and the computer. Table 4-1 identifies the data contained in each bit of the three receive monitor words. Receive monitor word 1 contains receiver frequency data, monitor word 2 contains receiver mode information, and monitor word 3 contains receiver squelch control information. Table 4-2 identifies the data contained in each bit of the three transmit monitor words. Transmit monitor words 1 and 2 also contain frequency and mode information, but monitor word 3 contains carrier level control information.

4-18. Logic Level Control Word Formats. One control word is transmitted on the logic level bus from the computer to the transmit control head and another control word services the receive control head. Table 4-3 identifies the data contained in each bit of these 32-bit words. The information in these control words is used primarily to light front panel indicators on the two control heads and the audio control unit.

4-19. CCCS BUS. The CCCS bus is the interface between the computer and the device control units (DCU) of the radio equipment controlled by the radio control group. This bus consists of three pairs of wire commonly called the carrier or clock bus, the control bus, and the monitor bus. The data transferred via these buses is in serial word formats, the composition of which is described in subsequent paragraphs. Data is transmitted from the computer to the DCU's of the various radio equipment by the control bus, and the monitor bus transfers data from the radio equipment to the computer. The carrier (clock) bus is driven by accessible memory card A7A6 timing for both the control and monitor buses. Figure 4-3 shows the phase relationship between the signals on the three buses and how the biphase modulated signals compare with an equivalent logic level representation. The following descriptions explain the functional character of the three bus signals.

Table 4-1. Receive Logic Level Monitor Words

BIT NO.	MONITOR WORD 1 (freq word)	MONITOR WORD 2 (mode word)	MONITOR WORD 3 (squelch word)
0	Logic 1	Logic 1	Logic 1
1	Not used	Receiver mute	Not used
2	10 MHz (2)	Not used	Master/slave
3	10 MHz (1)	Not used	Power interrupt
4	1 MHz (8)	*B2 channel data receive	Frequency initiate
5	1 MHz (4)	*B2 channel voice receive	Mode initiate
6	1 MHz (2)	*A2 channel data receive	Not used
7	1 MHz (1)	*A2 channel voice receive	Not used

Table 4-1. Receive Logic Level Monitor Words (Cont)

BIT NO.	MONITOR WORD 1 (freq word)	MONITOR WORD 2 (mode word)	MONITOR WORD 3 (squelch word)
8	100 kHz (8)	Not used	Not used
9	100 kHz (4)	Self test	Not used
10	100 kHz (2)	*B1 channel data receive	Not used
11	100 kHz (1)	Not used	Not used
12	10 kHz (8)	AME enable	Not used
13	10 kHz (4)	*B1 channel voice receive	Not used
14	10 kHz (2)	*A1 channel data receive	Not used
15	10 kHz (1)	*A1 channel voice receive	Not used
16	1 kHz (8)	Not used	B1 squelch (8)
17	1 kHz (4)	Not used	B1 squelch (4)
18	1 kHz (2)	Not used	B1 squelch (2)
19	1 kHz (1)	Not used	B1 squelch (1)
20	0.1 kHz (8)	Not used	A1 squelch (8)
21	0.1 kHz (4)	Power on	A1 squelch (4)
22	0.1 kHz (2)	Not used	A1 squelch (2)
23	0.1 kHz (1)	Not used	A1 squelch (1)

Note:

1. Not used indicates bit is transmitted as logic 0.
2. Numbers in parentheses indicate weighted bcd.

*3. Bits 4-5, 6-7, 10-13, and 14-15 of monitor word 2 function in pairs. A logic 1-0 in these bits select data 1, a 0-1 selects voice, a 1-1 selects data 2, and a 0-0 disables reception.

Table 4-2. Transmit Logic Level Monitor Words

BIT NO.	MONITOR WORD 1 (freq word)	MONITOR WORD 2 (mode word)	MONITOR WORD 3 (carrier level word)
0	Logic 1	Logic 1	Logic 1
1	Not used	Power off	Not used
2	10 MHz (2)	Vox enable	Master/slave
3	10 MHz (1)	Simplex enable	Power interrupt
4	1 MHz (8)	B1 channel transmit	Frequency initiate
5	1 MHz (4)	Logic 0	Mode initiate
6	1 MHz (2)	A1 channel transmit	Transceiver enable
7	1 MHz (1)	Logic 0	548U enable
8	100 kHz (8)	Receive through coupler	Power level change
9	100 kHz (4)	Self test	Servo enable
10	100 kHz (2)	B2 channel transmit	Not used
11	100 kHz (1)	Cw enable	Not used
12	10 kHz (8)	AME enable	Carrier level (8)
13	10 kHz (4)	Logic 0	Carrier level (4)
14	10 kHz (2)	A2 channel transmit	Carrier level (2)
15	10 kHz (1)	Logic 0	Carrier level (1)
16	1 kHz (8)	Logic 0	Not used
17	1 kHz (4)	Logic 0	Not used
18	1 kHz (2)	Medium power	Not used
19	1 kHz (1)	Low power	Not used
20	0.1 kHz (8)	Logic 0	Not used
21	0.1 kHz (4)	Filament on	Not used
22	0.1 kHz (2)	Plate on	Not used
23	0.1 kHz (1)	Key	Not used

Note: Numbers in parentheses indicate weighted bcd.

Table 4-3. Receive and Transmit Logic Level Control Words

BIT NO.	TRANSMIT CONTROL WORD	RECEIVE CONTROL WORD
0	A1 not used (logic 0)	A1 not used (logic 0)
1	A2 logic level address	A2 logic level address
2	A3 logic level address	A3 logic level address
3	A4 logic level address	A4 logic level address
4	A5 logic level address	A5 logic level address
5	A6 logic 0 } Subaddress group	A6 logic 0 } Subaddress group
6	A7 logic 1 }	A7 logic 1 }
7	Input/output identifier	Input/output identifier
8	Not used	Not used
9	Not used	Not used
10	Not used	Not used
11	Not used	Not used
12	Not used	Not used
13	Not used	Not used
14	Not used	Not used
15	Not used	Not used
16	Not used	Not used
17	Not used	Not used
18	Not used	Not used
19	Not used	Not used
20	Not used	Not used
21	Not used	Not used
22	Not used	Not used
23	Not used	Not used

Table 4-3. Receive and Transmit Logic Level Control Words (Cont)

BIT NO.	TRANSMIT CONTROL WORD	RECEIVE CONTROL WORD	
24	Not used	A1 channel receive audio	To audio control unit indicators
25	Not used	B1 channel receive audio	
26	Not used	A2 channel receive audio	
27	Keyed	B2 channel receive audio	
28	Self test prove	Self test prove	
29	Operate	Operate	
30	Frequency initiate	Frequency initiate	
31	Transmitter fault	Receiver fault	

Note:
1. When the bit 7 is logic 0, bits 8 through 31 are not used, and bits 1 through 6 have address of requested monitor word.
2. When bit 7 is logic 1, bits 1 through 6 contain the address of the control word, and bits 8 through 31 are as shown above.

4-20. Carrier (Clock) Bus. The carrier bus is a 4800-Hz sine-wave signal with a nominal 1-volt peak-to-peak (line-to-line) amplitude. This signal is generated by the hybrid bus driven on accessible memory card A7A6. Bit timing and word transfer rate on the control and monitor buses are controlled by this carrier signal.

4-21. Control Bus. The control bus contains 36-bit word intervals consisting of a 4-bit supervisory field followed by 32 bits of binary data (figure 4-3). The supervisory field is transmitted as carrier off and synchronizes the sine-wave data with the carrier bus signal. Data sine-wave signals in phase with the carrier (true) signal result in a logic 1, and data signals out of phase with the carrier (true) produce a logic 0. The sine-wave data on the control bus is applied to the control bus by the modulator section of accessible memory card A7A6.

4-22. As indicated in figure 4-3, each word transmitted on the control bus is composed of a dialogic bit (always logic 1), a 7-bit address field, and a 24-bit data field. The address field is divided into a 5-bit DCU address field and a 2-bit subaddress for second-level routing within the DCU. The first bit of the data field (bit 8) is the parity bit that is encoded so that bits 8 through 31 contain an even number of logic 1's. Bits 9 through 31 contain instructions that operate and/or control the radio equipment.

4-23. Monitor Bus. The monitor bus contains response words from the controlled radio equipment. These words are also transmitted in a 36-bit format as illustrated in figure 4-3 and are timed to follow the control word. However, the supervisory field is composed of four biphase logic 1's, instead of four bits of carrier off, and the dialogic bit is always a logic 0. The address field contains the same address as the associated control word. Information contained in the monitor word originates in the radio equipment. The associated DCU accepts digital data from the radio equipment, converts this digital data to biphase modulated sine-wave data, and transmits the data to the computer on the monitor bus.

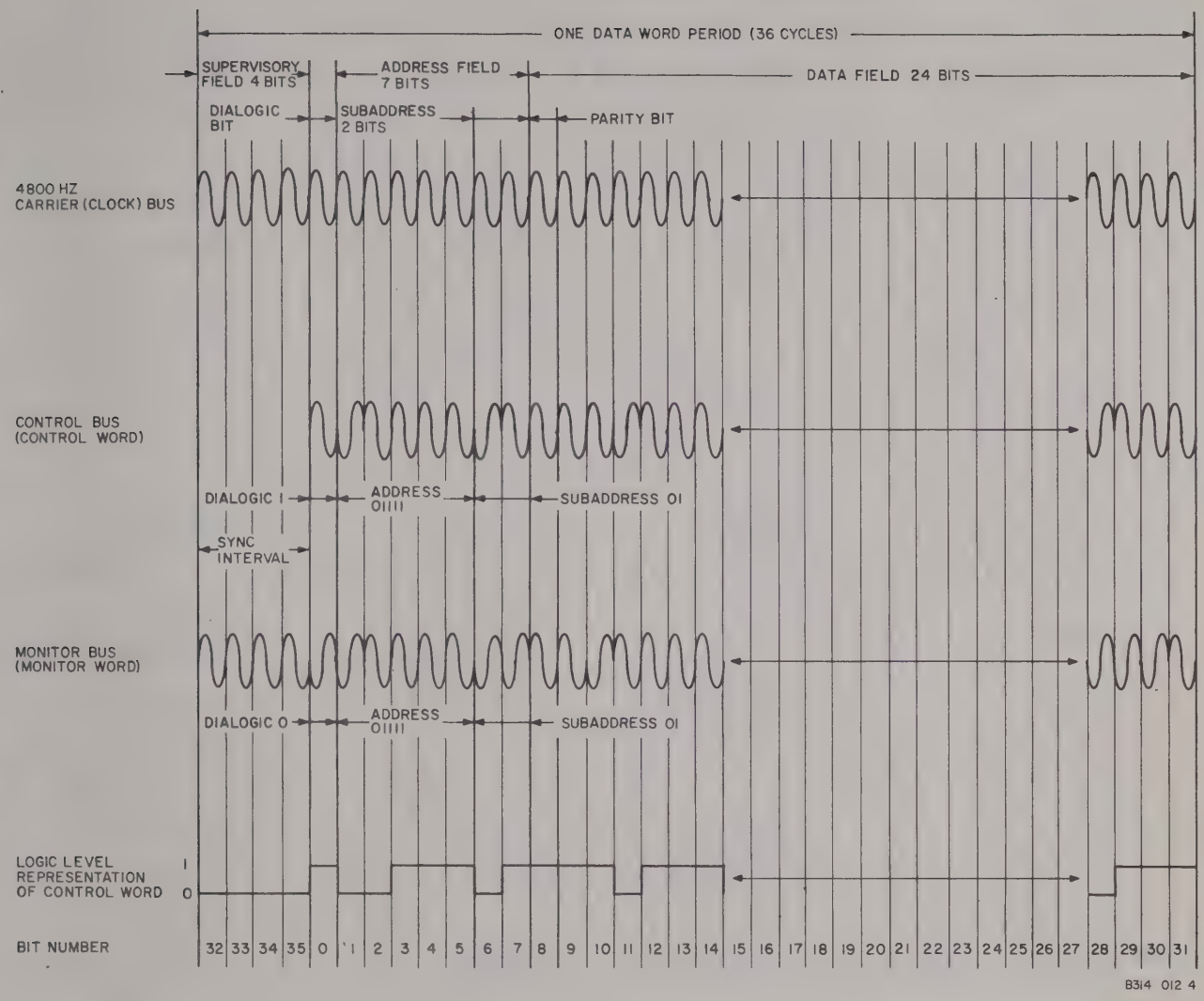


Figure 4-3. CCCS Bus Signal Relationship

4-24. CCCS Bus Control Word Formats. The radio receiver and transmitter are each controlled by four different 32-bit control words and the maintenance display is serviced by three similar control words. Tables 4-4 through 4-6 identify the data contained in each bit of these 11 control words.

4-25. Each control word transmitted by the computer on the CCCS control bus is addressed to a specific DCU by bits 1 through 5 of the control word (figure 4-3). Strapping on the DCU's permit the DCU to accept only those control words containing their unique address. Other DCU's on the control bus take no action on control words not containing their address. When a DCU recognizes its address in a control word, subaddress bits 6 and 7 (figure 4-3) route the information in the data field to the proper location in the device control functional elements (DCFE). The four possible subaddresses are represented in bits 6 and 7 as logic 0-0, 0-1, 1-0, and 1-1. Binary addresses of

Table 4-4. CCCS Bus Receiver Control Words

BIT NO.	CONTROL WORD 1 (freq word)	CONTROL WORD 2 (mode word)	CONTROL WORD 3 (squelch word)	CONTROL WORD 4 (mon request word)
0	Logic 1 (dialogic)	Logic 1 (dialogic)	Logic 1 (dialogic)	Logic 1 (dialogic)
1	(16)	(16)	(16)	(16)
2	(8)	(8)	(8)	(8)
3	(4) — 5-bit DCU address	(4) — 5-bit DCU address	(4) — 5-bit DCU address	(4) — 5-bit DCU address
4	(2)	(2)	(2)	(2)
5	(1)	(1)	(1)	(1)
6	Logic 0 — Subaddress	Logic 0 — Subaddress	Logic 1 — Subaddress	Logic 1 — Subaddress
7	Logic 0	Logic 1	Logic 0	Logic 1
8	Parity bit	Parity bit	Parity bit	Parity bit
9	Spare	Receiver mute	Logic 0	Logic 0
10	10 MHz (2)	Logic 0	Logic 0	Logic 0
11	10 MHz (1)	Logic 0	Logic 0	Logic 0
12	1 MHz (8)	*B2 channel data receive	Logic 0	Not used
13	1 MHz (4)	*B2 channel voice receive	Logic 0	Not used
14	1 MHz (2)	*A2 channel data receive	Logic 0	Not used
15	1 MHz (1)	*A2 channel voice receive	Logic 0	Not used
16	100 kHz (8)	Logic 0	Logic 0	Not used
17	100 kHz (4)	Self test	Logic 0	Not used
18	100 kHz (2)	*B1 channel data receive	Logic 0	Not used
19	100 kHz (1)	Logic 0	Logic 0	Not used
20	10 kHz (8)	Am enable	Logic 0	Not used

Table 4-4. CCCS Bus Receiver Control Words (Cont)

BIT NO.	CONTROL WORD 1 (freq word)	CONTROL WORD 2 (mode word)	CONTROL WORD 3 (squelch word)	CONTROL WORD 4 (mon request word)
21	10 kHz (4)	*B1 channel voice receive	Logic 0	Not used
22	10 kHz (2)	*A1 channel data receive	Logic 0	Not used
23	10 kHz (1)	*A1 channel voice receive	Logic 0	Not used
24	1 kHz (8)	Self-test low level	B squelch (8)	Not used
25	1 kHz (4)	Logic 0	B squelch (4)	Not used
26	1 kHz (2)	Logic 0	B squelch (2)	Not used
27	1 kHz (1)	Logic 0	B squelch (1)	Not used
28	0.1 kHz (8)	Logic 0	A squelch (8)	Not used
29	0.1 kHz (4)	Power on	A squelch (4)	Not used
30	0.1 kHz (2)	Logic 0	A squelch (2)	Not used
31	0.1 kHz (1)	Logic 0	A squelch (1)	Not used

Note:
1. Numbers in parentheses indicate weighted bdc.
2. Not used indicates logic 1's or 0's will function.
*3. Bits 12-13, 14-15, 18-21, and 22-23 of control word 2 function in pairs. A logic 1-0 in these bits select data 1, a 0-1 selects voice, a 1-1 selects data 2, and a 0-0 disables reception.

Table 4-5. CCCS Bus Transmitter Control Words

BIT NO.	CONTROL WORD 1 (freq word)	CONTROL WORD 2 (mode word)	CONTROL WORD 3 (carrier level word)	CONTROL WORD 4 (mon request word)
0	Logic 1 (dialogic)	Logic 1 (dialogic	Logic 1 (dialogic)	Logic 1 (dialogic)
1	(16)	(16)	(16)	(16)
2	(8)	(8)	(8)	(8)
3	(4) — 5-bit DCU address	(4) — 5-bit DCU address	(4) — 5-bit DCU address	(4) — 5-bit DCU address
4	(2)	(2)	(2)	(2)
5	(1)	(1)	(1)	(1)

Table 4-5. CCCS Bus Transmitter Control Words (Cont)

BIT NO.	CONTROL WORD 1 (freq word)	CONTROL WORD 2 (mode word)	CONTROL WORD 3 (carrier level word)	CONTROL WORD 4 (mon request word)
6	Logic 0	Logic 0	Logic 1	Logic 1
7	Logic 0 — Subaddress	Logic 1 — Subaddress	Logic 0 — Subaddress	Logic 1 — Subaddress
8	Parity bit	Parity bit	Parity bit	Parity bit
9	Spare	Power off	Logic 0	Logic 0
10	10 MHz (2)	VOX enable	Logic 0 (a/d inhibit)	Logic 0
11	10 MHz (1)	Simplex enable	A/d mux address (16)	Logic 0
12	1 MHz (8)	B1 channel transmit	A/d mux address (8)	Logic 0
13	1 MHz (4)	Logic 0	A/d mux address (4)	Logic 0
14	1 MHz (2)	A1 channel transmit	A/d mux address (2)	Logic 0
15	1 MHz (1)	Logic 0	A/d mux address (1)	Logic 0
16	100 kHz (8)	Receiver through coupler	Logic 0	Logic 0
17	100 kHz (4)	Self test	Logic 0	Logic 0
18	100 kHz (2)	B2 channel transmit	Logic 0	Logic 0
19	100 kHz (1)	Cw enable	Logic 0	Logic 0
20	10 kHz (8)	AME enable	Carrier level (8)	Logic 0
21	10 kHz (4)	Logic 0	Carrier level (4)	Logic 0
22	10 kHz (2)	A2 channel transmit	Carrier level (2)	Logic 0
23	10 kHz (1)	Logic 0	Carrier level (1)	Logic 0
24	1 kHz (8)	Logic 0	Logic 0	Logic 0
25	1 kHz (4)	Exciter tune	Logic 0	Logic 0
26	1 kHz (2)	Medium power	Logic 0	Logic 0

Table 4-5. CCCS Bus Transmitter Control Words (Cont)

BIT NO.	CONTROL WORD 1 (freq word)	CONTROL WORD 2 (mode word)	CONTROL WORD 3 (carrier level word)	CONTROL WORD 4 (mon request word)
27	1 kHz (1)	Low power	Logic 0	Logic 0
28	0.1 kHz (8)	Power amplifier tune	Logic 0	Logic 0
29	0.1 kHz (4)	Filament on	Logic 0	Logic 0
30	0.1 kHz (2)	Plate on	Logic 0	Logic 0
31	0.1 kHz (1)	Key	Logic 0	Servo enable

Note: Numbers in parentheses indicate weighted bcd.

Table 4-6. CCCS Bus Maintenance Display Control Words

BIT NO.	CONTROL WORD 1	CONTROL WORD 2	CONTROL WORD 3
0	Logic 1 (dialogic)	Logic 1 (dialogic)	Logic 1 (dialogic)
1	$\overline{(16)}$ logic 0 } Radio	$\overline{(16)}$ logic 0 } Radio	$\overline{(16)}$ logic 0 } Radio
2	(8) logic 1 } group	(8) logic 1 } group	(8) logic 1 } group
3	$\overline{(4)}$ logic 1 } Maintenance display address	$\overline{(4)}$ logic 1 } Maintenance display address	$\overline{(4)}$ logic 1 } Maintenance display address
4	(2) logic 1	(2) logic 1	(2) logic 1
5	(1) logic 1	(1) logic 1	(1) logic 1
6	$\overline{\text{Logic 0}}$ — Subaddress	$\overline{\text{Logic 1}}$ — Subaddress	$\overline{\text{Logic 0}}$ — Subaddress
7	$\overline{\text{Logic 0}}$	$\overline{\text{Logic 0}}$	$\overline{\text{Logic 1}}$
8	Parity bit	Parity bit	Parity bit
9	*Monitor data	Pwr ampl pwr interrupt	Spare
10	*Monitor data	Pwr ampl pwr fault summary	Spare
11	*Monitor data	Pwr ampl tune fault summary	Spare

Table 4-6. CCCS Bus Maintenance Display Control Words (Cont)

BIT NO.	CONTROL WORD 1	CONTROL WORD 2		CONTROL WORD 3
12	*Monitor data	Filament timer		Spare
13	*Monitor data	A/d complete		Spare
14	*Monitor data	A/d sign		Spare
15	*Monitor data	A/d overrange		Spare
16	*Monitor data	A/d output (8)	Hundreds	Spare
17	*Monitor data	A/d output (4)		Spare
18	*Monitor data	A/d output (2)		Spare
19	*Monitor data	A/d output (1)		Spare
20	*Monitor data	A/d output (8)	Tens	Spare
21	*Monitor data	A/d output (4)		Spare
22	*Monitor data	A/d output (2)		Display control fault
23	*Monitor data	A/d output (1)		Receiver control fault
24	*Monitor data	A/d output (8)	Units	Exciter control fault
25	*Monitor data	A/d output (4)		Power amplifier control fault
26	*Monitor data	A/d output (2)		Antenna coupler control fault
27	*Monitor data	A/d output (1)		Parity error control fault
28	*Monitor data	Spare		No response control fault
29	*Monitor data	Spare		Address error control fault
30	*Monitor data	Spare		Radio fault
31	*Monitor data	Spare		Operate

Note: 1. *Data contained in these bits is the equipment monitor data requested by bits 17 through 21 of the maintenance display monitor word.

Note: 2. Numbers in parentheses indicate weighted bcd.

Note: 3. Spare bits are transmitted as logic 0.

the radio equipment DCU's appearing in bits 1 through 5 are as follows:

Receiver DCU	0-1-0-0-1
Exciter DCU	0-1-0-1-0
Antenna coupler DCU	0-1-0-1-1
Power amplifier DCU	0-1-1-0-0
Power amplifier DCU 2 (548U analog)	0-1-1-1-0
Maintenance display DCU	0-1-1-1-1

4-26. CCCS Bus Monitor Word Formats. After a DCU recognizes an address directed to it, the data field is passed on to the radio equipment through the appropriate DCFE. The DCFE and/or the radio equipment decodes the control data and performs the required function (frequency change, mode select, etc.). A response is then generated by the DCFE and the radio equipment. This response constitutes bits 6 through 31 (figure 4-3) and is applied to the DCU. A dialogic bit (logic 0), the 5-bit address field, and 2-bit subaddress are added by the DCU to form the complete monitor word that is transmitted to the computer. Monitor words are generated in synchronism with the control bus, but the monitor word is delayed one bit by the integration period of the DCU. Tables 4-7 through 4-10 identify the information contained in each bit of the monitor words originated by the receiver, the transmitter, and the maintenance display.

Table 4-7. CCCS Bus Receiver Monitor Word

BIT NO.	MONITOR WORD 1
0	Logic 0 (dialogic)
1	(16) logic 0 — Radio group — 5-bit DCU address
2	(8) logic 1 — Radio group — 5-bit DCU address
3	(4) logic 0 — 5-bit DCU address
4	(2) logic 0 — 5-bit DCU address
5	(1) logic 1 — 5-bit DCU address
6	*Subaddress
7	*Subaddress
8	Parity error bit
9	Power interrupt
10	Power fault summary
11	Loop lock summary
12	Logic 0
13	**Logic 0 (low-level self-test fault)

Table 4-7. CCCS Bus Receiver Monitor Word (Cont)

BIT NO.	MONITOR WORD 1	
14	**Logic 0 (high-level self-test fault)	
15	Logic 0	
16	Tune complete	
17	9.9-kHz lock	Summed in bit 11
18	10-kHz lock	
19	9.9-MHz lock	
20	250-kHz lock	
21	243.71-kHz lock	
22	256.29-kHz lock	
23	Logic 0	
24	Logic 0	
25	Rf overload	
26	Receive rf translator out	
27	Agc monitor	
28	A1 channel receive audio	
29	B1 channel receive audio	
30	A2 channel receive audio	
31	B2 channel receive audio	

*Subaddress bits 6 and 7 are logic 0-0 in response to control word 1, logic 0-1 in response to control word 2, logic 1-0 for control word 3, and logic 1-1 for control word 4.

**Bits 13 and 14 are transmitted as logic 0 from the receiver and are modified by the computer program before transmission to the maintenance display.

Table 4-8. CCCS Bus Transmitter Power Amplifier Monitor Words

BIT NO.	1-KW PWR AMPLIFIER MONITOR WORD (responds to transmit control words 1, 2, and 4)	*1-, 2.5-, AND 10-KW PWR AMPLIFIER MONITOR WORD (responds to transmit control word 3)	2.5- AND 10-KW PWR AMPLIFIER MONITOR WORD (responds to transmit control words 1, 2, and 4)
0	Logic 0 (dialogic)	Logic 0 (dialogic)	Logic 0 (dialogic)
1	(16)	(16)	(16)
2	(8)	(8)	(8)
3	(4) — 5-bit DCU address	(4) — 5-bit DCU address	(4) — 5-bit DCU address
4	(2)	(2)	(2)
5	(1)	(1)	(1)
6	Subaddress	Subaddress	Subaddress
7	Subaddress	Subaddress	Subaddress
8	Parity error	Parity error	Parity error
9	Power interrupt	Power interrupt	Power interrupt
10	Plate current overload	Power fault summary	Power fault summary
11	Tune fault summary	Tune fault summary	Tune fault summary
12	Strapped to logic 0	Filament timer	Strapped to logic 0
13	Pwr ampl operate request	A/d complete	Power ampl operate request
14	Pwr ampl tune complete	A/d sign bit	Pwr ampl tune complete
15	Strapped to logic 0	A/d overrange indicator	Strapped to logic 0
16	Tune fault	A/d output (8) } Hundreds	Tune fault
17	Reflected power fault	A/d output (4) } Hundreds	Reflected power fault
18	Key monitor	A/d output (2) } Hundreds	Key monitor
19	Rf volt fault	A/d output (1) } Hundreds	Pwr ampl plate current fault

Table 4-8. CCCS Bus Transmitter Power Amplifier Monitor Words (Cont)

BIT NO.	1-KW PWR AMPLIFIER MONITOR WORD (responds to transmit control words 1, 2, and 4)	*1-, 2.5-, AND 10-KW PWR AMPLIFIER MONITOR WORD (responds to transmit control word 3)		2.5- AND 10-KW PWR AMPLIFIER MONITOR WORD (responds to transmit control words 1, 2, and 4)
20	Forward power	A/d output (8)		Pwr ampl screen current fault
21	Rf input	A/d output (4)	Tens	Rf input monitor
22	High-voltage monitor	A/d output (2)		Access plug interlock fault
23	Low-voltage monitor	A/d output (1)		Circuit breaker fault
24	Logic 0	A/d output (8)		Antenna interlock monitor
25	Logic 0	A/d output (4)	Units	Regulator monitor
26	Logic 0	A/d output (2)		Blower transfer
27	Logic 0	A/d output (1)		Servo error bit 2
28	Logic 0	Not used		Servo error bit 1
29	Logic 0	Not used		Tune sequence position A
30	Logic 0	Not used		Tune sequence position B
31	Logic 0	Not used		Tune sequence position C

*548U analog DCU has separate address. See paragraph 4-25.

Table 4-9. CCCS Bus Transmitter Exciter and Antenna Coupler Monitor Words

BIT NO.	EXCITER MONITOR WORD	ANTENNA COUPLER MONITOR WORD (490T-8)	ANTENNA COUPLER MONITOR WORD (490X-1)
0	Logic 0 (dialogic)	Logic 0 (dialogic)	Logic 0 (dialogue)
1	(16)	(16)	(16)
2	(8)	(8)	(8)

Table 4-9. CCCS Bus Transmitter Exciter and Antenna Coupler Monitor Words (Cont)

BIT NO.	EXCITER MONITOR WORD	ANTENNA COUPLER MONITOR WORD (490T-8)	ANTENNA COUPLER MONITOR WORD (490X-1)
3	(4)	(4)	(4)
4	(2)	(2)	(2)
5	(1)	(1)	(1)
6	Subaddress	Subaddress	Subaddress logic 1
7	Subaddress	Subaddress	Subaddress logic 1
8	Parity error	Parity error	Parity error
9	Power interrupt	Power interrupt	Power interrupt
10	Power fault summary	Power fault summary	Rf overvoltage
11	Loop lock summary	Tune fault summary	Tune fault summary
12	Coupler present	Coupler tune complete	Coupler tune complete
13	Logic 0	Logic 0	Logic 0
14	Logic 0	Logic 0	Logic 0
15	Transmit gain control monitor	Logic 0	Logic 0
16	Tune complete	Arc fault	*Sequence code A
17	9.9-kHz lock }	Tune fault	*Sequence code B
18	10-kHz lock }	Temperature fault	*Sequence code C
19	9.9-MHz lock } Summed	Transmit rf	Transmit rf
20	250-kHz lock } in bit 11	Spare	Series circuit in
21	243.71-kHz lock }	Spare	Phasing maximum
22	256.29-kHz lock }	Spare	Phasing minimum
23	Logic 0	Spare	Loading maximum
24	Logic 0	Spare	Loading minimum
25	Multiplex combiner output	Spare	6-ft closed

Table 4-9. CCCS Bus Transmitter Exciter and Antenna Coupler Monitor Words (Cont)

BIT NO.	EXCITER MONITOR WORD	ANTENNA COUPLER MONITOR WORD (490T-8)	ANTENNA COUPLER MONITOR WORD (490X-1)
26	Transmit rf transmitter output	Spare	6-ft open
27	Transmit if. amplifier output	Spare	4-ft closed
28	A1 channel transmit if.	Spare	4-ft open
29	B1 channel transmit if.	Spare	1.5-ft closed
30	A2 channel transmit if.	Spare	1.5-ft open
31	B2 channel transmit if.	Spare	Key interlock closed

*Tune sequence code is defined as follows:

BIT 16 (A)	BIT 17 (B)	BIT 18 (C)	TUNE STEP
1	0	0	1-tune start
1	1	0	2-home
1	1	1	3-receive
0	1	1	4-preposition
0	0	1	5-tune
0	0	0	6-operate
0	1	0	Illegal
1	0	1	Illegal

Table 4-10. CCCS Bus Maintenance Display Monitor Word

BIT NO.	MAINT DISPLAY MONITOR WORD	
0	Logic 0 (dialogic)	
1	(16)	5-bit DCU address
2	(8)	
3	(4)	
4	(2)	
5	(1)	

Table 4-10. CCCS Bus Maintenance Display Monitor Word (Cont)

BIT NO.	MAINT DISPLAY MONITOR WORD
6	Subaddress — Same as control word causing transmission
7	Subaddress
8	Parity result
9	Power interrupt
10	Logic 0
11	A/d mux address (16)
12	A/d mux address (8)
13	A/d mux address (4)
14	A/d mux address (2)
15	A/d mux address (1)
16	Radio control self-test enable
17	Antenna coupler display request
18	Receiver display request
19	Exciter display request
20	Pwr amplifier display request
21	Pwr amplifier analog display request
22	Spare
23	Spare
24	Spare
25	Spare
26	Spare
27	Spare
28	Spare
29	Spare
30	Spare
31	Spare

4-27. RECEIVE AND TRANSMIT CONTROL HEADS. Front panels A8A4 and A7A9 of the receive and transmit control heads figure (4-1) are computer entry panels that provide the operator interface to the radio set. At these panels, the operator can input frequency and mode control commands to the computer to control the radio equipment and can monitor the radio status by observing front panel indicators. These control commands are generated by positioning switches on the front panels. The switches manually set the appropriate condition (logic 1 or logic 0) in the bit positions of the logic level receive and transmit monitor words. Wiring from the front panel switches and indicators is cabled to two female connectors that mate with jacks J1 and J2 of matrix cards A8A2 and A7A7. The only exception to this wire routing is the interlock circuits of the transmit control head that are wired from the front panel directly to jack A7A10J1 on the rear panel. The matrix cards, logic level slave cards, and the backplane cards in both control heads are identical printed circuit boards. Plug P1 of the matrix cards mates with jack J2 of the backplanes, and all other circuit cards plug into the respective backplanes. Circuit tracks of the backplane cards serve as interconnect wiring for all circuits of the associated control heads. All inputs and outputs of the control heads are from power and signal connectors on the rear panels. A third connector on each rear panel is used for address strapping in the computer program. Wiring from the rear panel to the backplanes is cabled to plugs that mate with jack J1 on the backplane cards.

4-28. Rear panel connectors A8A5J1 and A7A10J1 connect to pendant cables of the audio control unit. Internal strapping in the audio control unit connects the receive control head to the computer via connector A7A10J1, backplane card A7A8, and the logic level bus. The signal path between the computer and the radio DCU is via the CCCS bus that leaves the computer at the modulator section of accessible memory card A7A6, and is routed through backplane card A7A8, rear panel connector A7A10J1, filters FL3, FL4, and FL5, in the audio control unit, and connector J1 to the DCU.

4-29. Matrix Cards A8A2 and A7A7. Matrix cards A8A2 and A7A7 (figure 4-1) contain the circuits that interface the front panel controls and indicators with the logic level bus. Parallel digital information is set into six 4-bit shift registers from the front panel switches. Digital information in these registers is then read out serially and constitutes the 24-bit logic level monitor word data field. This readout occurs when a request is received from the computer. A diode and resistor network on the circuit card routes front panel switch data to multiple inputs of the shift registers, and allows identical circuit cards to be used in both the transmit and receive control heads. When the front panel switches apply ground to the shift registers through the diode network, a logic 0 is set in the corresponding bit position of the shift register. The absence of ground enables resistive pull-up circuits and a logic 1 is set in the applicable bit position of the shift registers.

4-30. Logic Level Slave Cards A7A1 and A8A1. Logic level slave cards A7A1 and A8A1 contain registers that store logic level control words addressed to the respective control heads by the computer. The card also has lamp driver circuits that light front panel indicators to reflect the status of the radio equipment. Other circuits provide address decoding, timing, word enable functions, and the logic level interface between the front panels and the computer.

4-31. Hardwire Memory Card A7A2. Hardwire memory card A7A2 contains the control program that determines the overall activity of the radio control group. The control program consists of 16-bit words that are stored in semiconductor read only memory modules. The memory modules are parallel addressed by an instruction address counter and each instruction is read serially into instruction decode card A7A5.

4-32. CCCS Timing Card A7A3. The primary function of CCCS timing card A7A3 is to generate the frame timing that controls the transmission and reception of control and monitor words on the CCCS bus. Other circuits on the card function as an address selector, an address serializer, a timing counter, and a fault detector.

4-33. Processor Card A7A4. Processor card A7A4 provides the internal timing for the computer. There are three steps in the basic processor timing cycle: shifting the instruction data from the hardwire memory to the instruction decode card, shifting the accessible memory data through gates that are enabled by circuits of the instruction decode card, and advancing the program to the next required instruction.

4-34. Instruction Decode Card A7A5. Instruction decode card A7A5 stores and decodes the instruction data received from hardwire memory card A7A2, and routes data stored in accessible memory card A7A6 according to the instructions that are processed. The instruction decode circuits also determine what data is placed in the accessible memory, permit the computer to set up arbitrary data fields, and make decisions pertaining to the data contained in accessible memory locations. The instruction data is verified by reading each instruction from the hardwire memory twice and comparing the two readings. If the comparison is negative, circuits of processor card A7A4 automatically resets the program to the first step.

4-35. Accessible Memory Card A7A6. Accessible memory card A7A6 is a serial in/serial out register array consisting of 16 storage locations, 32 bits in length. These locations provide storage for control data that is to be transmitted or monitor data that is to be analyzed. Data contained in these storage locations is under the computer program control. The modulator, demodulator, and oscillator for the CCCS bus are also part of this card.

4-36. AUDIO CONTROL UNIT. The audio control unit (figure 4-1) is the operating section of the radio control group. Only the SIMPLEX/DUPLEX and the VOX-CW/PTT switches on the front panel are used for control of the radio equipment. The remaining subassemblies and accessories of the audio control unit function in the operation of the radio equipment after it has been tuned and set up for operation by the receive and transmit control heads. The SIMPLEX/DUPLEX switch manually controls the status of bit 11 in CCCS bus transmitter control word 2 (table 4-5). When the switch is open (in the DUPLEX position), a logic 1 is set in bit 11 enabling duplex operation. In the SIMPLEX position, a ground (logic 0) is set in bit 11 of transmit control word 2 and simplex operation is enabled. The VOX-CW/PTT switch controls the content of bit 10 in CCCS bus transmit control word 2 (table 4-5) by applying or removing ground in the same manner as the SIMPLEX/DUPLEX switch. A logic 0 enables the vox circuits of the radio exciter, and a logic 1 enables the cw and push-to-talk key circuits.

4-37. Receive Circuits. Figure (4-1) shows six audio inputs applied to line amplifier A5 through connector J1 of the audio control unit. These inputs include independent-sideband channels A1, A2, B1, and B2, a monitor bus, and an order wire. Front panel switches permit the operator to select one or more of these audio channels for monitoring by an external headset or by speaker LS1 as determined by the setting of switch S7. When the audio is monitored by the speaker, additional amplification is provided by speaker amplifier A6.

4-38. Transmit Circuits. Transmissions from the radio control group are made by an external push-to-talk desk or headset microphone connected to jack J3 or by an external cw key connected to jack J4. Selection of the type of keying is made by front panel switches on the transmit control head and the audio control unit. Audio transmitted from the external microphone is routed through mike amplifier A4, agc amplifier A3, and line amplifier A2 to the four independent-sideband channels and the order wire. Front panel switches enable the operator to select one or combinations of these channels for audio transmissions.

4-39. Power Distribution. Primary power (120 volts ac) is applied to the radio control group through connector J2 of the audio control unit. Filters FL1 and FL2 connected in series with the ac lines filter undesired signals from the power lines. Circuit breaker CB1 provides overload protection for the 120-volt ac circuit applied to terminal board TB1, and is also a front panel ON/OFF switch. On the terminal board, the 120-volt ac power is divided into two circuits. One circuit is applied to dimmer resistor R42 that adjusts the brilliance of the front panel edge lighting on the receive and transmit control heads and the audio control unit. The second circuit is routed to fan B1 and power supplies PS1, A7A10PS1, and A8A5PS1. Power supply PS1 provides 24 volts dc for operation of amplifiers A2, A3, A4, A5, and A6 in the audio control unit; power supplies A7A10PS1 and A8A5PS1 supply the dc voltages for operation of the logic circuits and front panel indicators of the transmit and receive control heads. Both ac circuits are applied to the two control heads through pendant cables of the audio control unit. Plugs on these cables mate with connector J2 on the rear panel of the respective control heads.

SECTION II

FUNCTIONAL OPERATION OF ELECTRONIC CIRCUITS

4-40. GENERAL.

4-41. This section provides detailed descriptions of the control and indicator circuits on the front panels of the transmit and receive control heads, matrix card circuits, logic level slave card circuits, the five circuit cards that make up the rom computer and the audio and power circuits of the audio control unit. Simplicity of the remaining circuits renders detailed descriptions unnecessary. For principles of operation of basic standard circuits, refer to T.O. 31-1-141.

4-42. TRANSMIT AND RECEIVE CONTROL HEAD FRONT PANEL CONTROL CIRCUITS.

4-43. The transmit and receive control head front panels, shown as blocks A7A9 and A8A4 in figure 4-1, consist of switches, indicators, and wiring that is represented schematically in figures 7-1 and 7-2. The physical and functional characteristics of these two panels are similar, but contain minor differences explained in the following descriptions.

4-44. TRANSMIT CONTROL HEAD FRONT PANEL CIRCUITS. Refer to figure 7-1. The ground bus (P1-37), the 4.7-volt dc bus (P2-47), and the three monitor word enable signals applied to P2-49, P1-2, and P1-1 provide the basis for the functions of the front panel circuits. The 4.7 volts dc is applied to all the front panel indicator lamps through LAMP DIM rheostat R1 that varies the brilliance of the indicators. This dc bus is also extended to the six L2 terminals of FREQUENCY-MHZ switch S10 to light the numbers selected by the six decade thumbwheels. The indicator lamps of switch S10 are an integral part of the printed-circuit switch assembly and are not shown in figure 7-1. A dc return path for the switch indicator lamps is provided by the internal strapping of the L1 terminals of switch S10 to the ground bus. Therefore, the indicator lamps in switch S10 are lighted to the level of brilliance determined by rheostat R1 at all times when 4.7 volts dc is present at P2-47. This condition also applies to UNIT PWR indicator DS2 that has its terminals permanently wired to the ground and 4.7-volt dc buses through LAMP DIM resistor R1. The remaining indicators FAULT (DS1), OPR (DS3), PROVE (DS4), KEYED (DS5), and INITIATE (DS6) are wired to the 4.7-volt dc bus through LAMP DIM resistor R1, but must have a dc return path applied externally through pins P2-17, P1-6, P1-33, P1-31, and P1-5 respectively before they are lighted. These dc return paths are completed by lamp driver circuits of logic level slave card A7A1 (figure 4-1) in response to the transmit logic level control word (table 4-3) or when activated manually by LAMP TEST switch S4. When switch S4 is held pressed, all the transmit control head indicator lamps are checked by the application of ground to P1-35. This ground is extended to the logic level slave card to activate the lamp driver circuits that provide a dc return path for all the indicators through their respective P1 and P2 pin connections shown in figure 7-1. The auxiliary branch of the 4.7-volt dc bus extended to P2-45 is provided to light and control the brilliance of indicator lamps external to the radio control group. This bus is routed to the rear panel of the transmit control head but is not used.

4-45. Switches on the transmit control head front panel are all wired to either the ground bus or to one of the three monitor word enable inputs. These switches either apply or remove ground to activate the functions indicated on the output pins of connectors P1 and P2 shown in figure 7-1. FREQUENCY MHZ switch S10 is a 6-section (A through F) printed circuit thumbwheel switch assembly. Each section of the switch applies bcd weighted outputs determined by the numbers selected when the thumbwheels are rotated. The bcd outputs determine the bit status of bits 2 through 23 of transmit logic level monitor word 1 (table 4-2). Sections B, C, D, E, and F of switch S10 are full-decade selectors, but section A is limited to digits 0, 1, and 2. For this reason, bcd weighted outputs 8 and 4 of section A are not used. When any of the thumbwheels of switch S10 are repositioned, ground is applied to P1-4. This ground is extended through matrix card A7A7 to logic level slave card A7A1 (figure 4-1). Lamp driver circuits on the logic level slave card are activated and a dc return path for INITIATE indicator DS6 is provided through P1-5, lighting the indicator lamp.

4-46. Repositioning the thumbwheels of switch S10 does not cause transmission of the bcd data selected by the six sections of the switch. Momentarily pressing INITIATE pushbutton indicator switch S11 applies a frequency initiate ground to P2-19 and a logic 1 is set in bit 4 of transmit logic level monitor word 3 (table 4-2). The presence of a logic 1 in this bit position causes the computer to request a readout of transmit logic level monitor words 1 and 2 (table 4-2). In order to do this, the data set up by the switches on the transmit control head front panel is parallel loaded into six 4-bit shift registers on matrix card A7A7 (figure 4-1). This readout occurs in word 3, 2, 1 (carrier level word, mode word, and frequency word) sequence and is timed by the application of monitor word 3 enable at P1-1, monitor word 2 enable at P1-2, and monitor word 1 enable at P2-49. After switch S11 has been pressed, INITIATE indicator DS6 goes out unless a power interrupt, power fault, or tune fault is detected by the presence of a logic 1 in bits 9, 10, or 11 of any of the CCCS bus transmitter monitor words (tables 4-8 and 4-9).

4-47. SELF TEST/AM/CW switch S7 is a 5-position switch that selects transmitter 4-channel independent-sideband operation, independent-sideband self-test operation, AME operation, or cw operation on either channel A1 or B1. When the switch is in the independent-sideband position as shown in figure 7-1, switches S5, S6, S8, and S9 are enabled. These switches control the on/off operation of independent-sideband channels A1, A2, B1, and B2. Movement of any of the independent-sideband switches or switch S7 applies a momentary mode inititate signal to P2-46. This action changes the condition of bit 5 of transmit logic level monitor word 3 (table 4-2) indicating to the computer that new mode information is available. At the same time, contacts 1 and 2 of the respective independent-sideband switches apply the monitor word 2 enable (logic 0 when a request for a monitor word is transmitted by the computer) present at P1-2 to their respective outputs at P2-29, P2-30, P2-35, and P1-29. These outputs enable or disable the indicated sideband channel by controlling the bit condition (logic 1 or logic 0) of bits 4, 6, 10, and 14 of transmit logic level monitor word 2 (table 4-2).

4-48. When switch S7 is set to the SELF TEST position, the four independent-sideband switches remain enabled but contacts 7 through 11 of switch S7B provide the momentary initiate signal to pin P2-46. The monitor word 2 enable (logic 0) at P1-2 is extended to P2-37 by contacts 2 and 6 of switch S7A. This logic 0 is then used to set the condition of bit 9 in transmit logic level monitor word 2 (table 4-2). A logic 1 in this bit causes the computer to initiate the transmitter self-test routine. During the self-test routine, the availability of the four independent-sideband channels depends upon the position (ON or OFF) of switches S5, S6, S8, and S9.

4-49. AME operation is selected by setting switch S7 to the AM position. In this position, the four independent-sideband switches are disabled and the movement of switch S7B provides the momentary mode initiate signal at P2-46. The monitor word 2 enable (logic 0) at P1-2 is applied to P1-24 through contacts 6 and 3 of switch S7A, and controls AME enable by setting the condition of bit 12 in transmit logic level monitor word 2 (table 4-2).

4-50. Cw operation is selected by setting switch S7 to CW A1 and CW B1. In either of these positions, a momentary mode initiate signal is applied to P2-46; a logic 0 is available at P1-2 and is switched to P2-28 as a cw enable signal and to either P2-29 or P2-30 as an A1 or B1 transmit channel enable signal. The CW A1 position of switch S7 controls the condition of bits 6 and 11 of transmit logic level monitor word 2, and the CW B1 position controls the condition of bits 14 and 11 (table 4-2). A cw interlock circuit is operated by pins 1 through 6 of switch S7B. The cw interlock A, B, and common lines are wired directly to connector J1 on the rear panel of the transmit control head. Strapping at this connector provides continuity between cw A and cw common when switch S7 is set to CW A1 or CW B1, and continuity between cw B and cw common when switch S7 is in any other position. This interlock circuit is used in conjunction with the key control and key interlock circuits described in paragraph 4-53. Section C of switch S7 is wired in conjunction with switch S3 and enables full-carrier suppression when either cw position is selected.

4-51. Carrier level switch S3 selects the carrier level when the transmitter is in the independent-sideband mode of operation. Section C of the switch provides the momentary mode initiate when the switch is repositioned, and sections A and B switch the monitor word 3 enable (logic 0) and provide binary weighted outputs to transmit logic level monitor word 3 (table 4-2). The following list indicates the bits of transmit logic level monitor word 3 that are controlled by switch S3 to produce the desired carrier attenuation.

CARRIER LEVEL	BIT 12	BIT 13	BIT 14	BIT 15
0 dB (maximum carrier)	0	0	0	0
-3 dB	0	0	0	1
-6 dB	0	0	1	0
-9 dB	0	0	1	1
-12 dB	0	1	0	0
-15 dB	0	1	0	1
-18 dB	0	1	1	0
-21 dB	0	1	1	1
-24 dB	1	0	0	0
-27 dB	1	0	0	1
-30 dB	1	0	1	0
OFF (full-carrier suppression)	1	1	0	0

4-52. Transmit power switch S1 controls the primary power to all elements of the transmitter except the DCU and DCFE power. The switch also selects the rf output power level of the transmitter. Movement of switch S1 causes a momentary interruption of the ground applied to P1-3. This action enables circuits of logic level slave card A7A1 (P1-35, figure 7-5) and causes INITIATE indicator DS6 to light but does not cause the computer to read transmit logic level monitor words 3 and 2. When switch S1 is changed from OFF to STBY or from STBY to OFF, ground is applied or removed at P1-28. This action enables circuits of matrix card A7A7 (J1-28, figure 7-3) that change the mode initiate bit of transmit logic level monitor word 3 (table 4-2) and causes the computer to send the new mode data to the applicable DCU's of the transmitter equipment. The following list indicates the bits of transmit logic level monitor word 2 that are controlled by switch S1 to apply or remove transmitter power and to select the desired rf output.

SWITCH POSITION	BIT 1	BIT 18	BIT 19	BIT 21	BIT 22
OFF	1	0	0	0	0
STBY	0	0	0	1	0
HIGH	0	0	0	1	1
LOW	0	0	1	1	1

4-53. Switch S2 controls the key and key interlock circuits of the transmitter. When the switch is in the KEY position, ground is applied to P2-33 providing that switch S1 is set to either HIGH or LOW. This output controls the condition of bit 23 of transmit logic level monitor word 2 (table 4-2). A logic 1 in this bit causes the transmitter to be keyed continuously via the CCCS bus. When switch S2 is set to OFF, bit 23 is changed to logic 0 and the CCCS bus key is disabled. The key interlock A and B outputs and the VOX interlock circuit are wired directly to connector J1 on the rear panel of the transmit control head. Continuity between key interlock A and key interlock B is provided when switch S2 is set to VOX/PTT and switch S1 is set to LOW or HIGH. Strapping in the audio control unit provides continuity between key interlock A and cw common. The VOX interlock and key interlock B circuits operate in conjunction with the VOX-CW/PTT switch and the cw key or microphone ptt key on the audio control unit to select either VOX or cw/ptt keying, and prevent keying the transmitter unless it is operating on either high or low power.

4-54. The dimmed 120 volts ac applied to the transmit control head panel edge lighting originates in the audio control unit. This voltage lights the front panel switch and indicator labels to a level of brilliance controlled by the DIM control on the audio control unit.

4-55. RECEIVE CONTROL HEAD FRONT PANEL CONTROL CIRCUITS. Refer to figure 7-2. Circuits of the receive control head front panel are fundamentally the same as those described for the transmit control head in paragraphs 4-44 through 4-53. The FREQUENCY-MHZ switch in both heads are identical. Indicator lamp circuits are similar except that the receive control head does not have a KEYED indicator. This configuration changes the designation of the INITIATE indicator to DS5 as shown in figure 7-2, but the function of indicators DS1 through DS5 are the same as corresponding indicators on the transmit control head.

4-56. When any of the thumbwheels of switch S10 are repositioned, INITIATE indicator DS5 is lighted in the same manner as described for the transmit control head. When INITIATE switch S11 is pressed momentarily, the frequency initiate ground applied to P2-19 causes a logic 1 to be set in bit 4 of receive logic level monitor word 3 (table 4-1). The logic 1 in this bit causes the computer to request a readout of receive logic level monitor words 1 and 2 (table 4-1). In order to do this, the data set up by the switches on the receive control head front panel is parallel loaded into six 4-bit registers on matrix card A8A2 (figure 4-1). This readout occurs in word 3, 2, 1 (squelch word, mode word, and frequency word) sequence and is timed by the application monitor word 3 enable at pin P1-1, monitor word 2 enable at pin P1-2, and monitor word 1 enable at pin P2-49. After switch S11 has been pressed, INITIATE indicator DS5 goes out unless a power interrupt power fault, address error, computer power fault, or a tune fault is detected by the presence of a logic 1 in bits 9, 10, or 11 of the CCCS bus receiver monitor word (table 4-7).

4-57. SELF TEST/AM/SELF TEST switch S7 is a 4-position switch that selects receiver 4-channel independent-sideband operation, independent-sideband self-test operation, AME operation, and amplitude modulation self-test operation. These modes of receiver operation are selected by controlling the condition of bits 9 and 12 of receive logic level monitor word 2 (table 4-1). Any repositioning of switch S7 causes the mode and squelch data in logic level monitor words 2 and 3 to be transmitted to the receiver. The following list indicates the bit conditions required to select the four modes of receiver operation.

SWITCH POSITION	BIT 9	BIT 12
Independent sideband	0	0
Independent-sideband SELF TEST	1	0
AM	0	1
AM SELF TEST	1	1

4-58. When switch S7 is in the independent sideband or the independent-sideband SELF TEST position, channel switches S5, S6, S8, and S9 are enabled and provide data outputs for receiver channels A1, A2, B1, and B2 as shown in figure 7-2. Each of the four channel switches turn the associated channel OFF, or select VOICE, DATA 1, or DATA 2 receiver operation. These functions are selected by controlling the condition of eight bits in receive monitor word 2 (table 4-1). The following list indicates the bits associated with each of the four receive channels and the condition of the bits required to select the four receiver functions of each channel.

Switch Position	Channel A1 Bits 14-15	Channel A2 Bits 6-7	Channel B1 Bits 10-13	Channel B2 Bits 4-5
OFF	0 - 0	0 - 0	0 - 0	0 - 0
VOICE	0 - 1	0 - 1	0 - 1	0 - 1
DATA 1	1 - 0	1 - 0	1 - 0	1 - 0
DATA 2	1 - 1	1 - 1	1 - 1	1 - 1

4-59. When any of the mode control switches (S5 through S9) are repositioned, a momentary mode initiate signal is applied to P2-46 and sets a logic 1 in bit 5 of receive logic level monitor word 3. A logic 1 in this bit position indicates that new mode information is available and causes the computer to request a readout of monitor word 2. This readout is accomplished by sequentially applying a monitor word 3 enable at P1-1 and a monitor word 2 enable at P1-2.

4-60. RCVR PWR switch S1 controls the on/off operation of primary power to all the receiver equipment except the DCU's and DCFE's. This operation is controlled by bit 21 of receive logic level monitor word 2 (table 4-1). A logic 0 in this bit turns the receiver power off and a logic 1 turns the power on. When switch S1 is repositioned, the content of bit 21 is extended through P1-14 and a mode initiate signal at P2-46 causes a readout of receive logic level monitor words 3 and 2.

4-61. Squelch switches S2 and S3 vary the squelch level of independent-sideband channels A1/A2 and B1/B2. Outputs of the two switches are weighted bcd and are available only when a monitor word 3 enable is present at P1-1. These bcd outputs shown in figure 7-2 control the condition of bits 16 through 23 of receive logic level monitor word 3 (table 4-1). When either squelch switch is repositioned, a logic 1 is set in bit 5 of logic level monitor word 3 causing the mode and squelch data in logic level monitor words 2 and 3 to be transmitted to the receiver. The relationship between squelch switches S2 and S3 and their respective bit conditions in receive logic level monitor word 3 is as follows:

	SQUELCH A (S3)					SQUELCH B (S2)				
SWITCH POSITION	BITS	20	21	22	23	BITS	16	17	18	19
9 (maximum squelch)		0	0	0	0		0	0	0	0
8		0	0	0	1		0	0	0	1
7		0	0	1	0		0	0	1	0
6		0	0	1	1		0	0	1	1
5		0	1	0	0		0	1	0	0
4		0	1	0	1		0	1	0	1
3		0	1	1	0		0	1	1	0

SWITCH POSITION	SQUELCH A (S3) BITS	20 - 21 - 22 - 23	SQUELCH B (S2) BITS	16 - 17 - 18 - 19
2		0 - 1 - 1 - 1		0 - 1 - 1 - 1
1 (minimum squelch)		1 - 0 - 0 - 0		1 - 0 - 0 - 0
OFF		1 - 0 - 0 - 1		1 - 0 - 0 - 1

4-62. The receive control head panel edge lighting is identical to that of transmit control head described in paragraph 4-54.

4-63. MATRIX CIRCUITS.

4-64. The transmit and receive control head matrix cards shown as blocks A7A7 and A8A2 in figure 4-1 provide the interface between the respective front panels and the backplane cards. Identical matrix cards are used in both control heads. The following description of the matrix card circuits is keyed to the detailed logic diagram shown in figure 7-3.

4-65. All the connections between the front panel controls and indicators and the matrix circuits are made through connectors J1 and J2 and the required interface with the backplane card is via blueline connector P1. Seventeen functions of the front panel controls are directly connected between pins of connectors J1 and J2 to pins of connector P1 and serve no purpose in the operation of the matrix circuits. Examples of these through connections are the front panel key and lamp bus functions at pins 33 and 45 of connector J2 and the lamp test 1 and frequency switch change functions at pins 35 and 4 of connector J1.

4-66. The primary function of the matrix circuits is to set the condition (logic 1 or logic 0) of the 24 bits in the three logic level monitor words. The data composition of these words is described in tables 4-1 and 4-2. Because the same matrix cards are used in both the transmit and receive control heads, the transmit and receive control functions are shown at pins of connectors J1, J2, and P1. These functions originate at the control head front panels, the radio equipment, or the audio control unit, and are routed through gates and diode-resistor networks (figure 7-3) to the parallel inputs of 4-bit shift registers A2, A3, A4, A6, A7, and A8. The shift registers are connected as parallel in/serial out arrays that store and readout the 24 data bits of the logic level monitor words. The monitor word data in the shift registers is determined by the monitor word enable inputs applied to the transmit and receive control head front panel switches and gates A1, A5, A13, and A11D. A logic 0 applied to parallel input pins 5, 3, 2, and 14 of the shift registers sets a logic 0 in the associated bit position when strobed in a parallel mode. The absence of ground at these inputs enables the resistive pull-up networks and sets a logic 1 in the associated bit position. There are two types of parallel inputs to the six shift registers. The first type is routed directly from the pins of connectors J1 and J2 through steering diodes to the register inputs. The second type is gated from the input pins of connector P1 and J2 through the steering diodes to the register inputs. These gated inputs are applied to the register only when a monitor word 3 enable or a monitor word 2 enable signal is also applied to the gates.

4-67. A logic 0 (ground) is normally present at J2-46. When any of the switches on the transmit and receive control heads, except FREQUENCY-MHZ switch S10 and XMIT PWR switch S1, are repositioned, the logic 0 is removed momentarily (figures 7-1 and 7-2). During this interval, a mode initiate logic 1 is applied to the input of NAND gate A16C, and the logic 0 output sets the flip-flop formed by gates A12A and A11B. The resulting output logic 1 is inverted by gate A1A if a monitor word 3 enable is also applied to gate A1A. Assuming that a logic 1 is present at pins 1 and 2 of gate A1A, a logic 0 is applied to pin 3 of shift register A7 through diode CR37. This pin is the input to bit 5 of logic level monitor word 3 (tables 4-1 and 4-2). When a logic 0 is set in this bit

(a logic 1 after inversion by A16D), the computer is advised that a mode change has been made in the front panel switches or that computer entries through connector P1 have altered the transmitter or receiver operational mode.

4-68. Figure 7-3 illustrates how the condition of some of the bits of the monitor words are controlled by inputs from connector P1, rather than from the front panels through connectors J1 and J2. The 548U enable at P1-13 is a transmitter function only. A monitor word 3 enable signal (ground) at this input is applied or removed by manually positioning 548U/208U switch A7A10 S1 on the rear panel of the transmit control head. This switch is set to the 208U position when a 2.5- or a 10-kW transmitter is controlled by the transmit control head. When the switch is set to the 548U position, control and monitoring for the 1-kW transmitter analog adaptor slice, which has an independent DCU, is enabled. This function is accomplished as the switch applies logic 0 (ground) to pin 14 of shift register A7 through P1-13 and diode CR68. (See bit 7, table 4-2.) Switch A7A10S1 is not normally changed during operation.

4-69. The simplex and VOX inputs at P1-D and P1-3 originate at the SIMPLEX/DUPLEX and VOX-CW/PTT switches on the audio control unit. Logic 0 applied to these inputs is inverted by gates A14A and A14C and are applied to pins 2 and 14 of shift register A2 through gates A1B, A5A, and associated diodes CR2 and CR8. (See bits 2 and 3, table 4-2.) In the VOX function, gates A15D, A9A, and the series connected capacitors C5 and C8 are one-shot multivibrators that trigger multiple input NAND gate A10. The logic 1 output of gate A10 is then inverted by gate A11A to provide the logic 0 required to set the mode initiate flip-flop. The two one-shot multivibrators provide separate inputs at pins 2 and 9 of gate A10 to ensure that the mode initiate flip-flop is set when the VOX enable ground is applied to P1-3 and when the cw/ptt is enabled by removing the ground at P1-3. Gates A15B and A9C along with capacitors C2 and C3 trigger the mode initiate flip-flop in a similar manner when simplex and duplex operation is selected by applying or removing ground at P1-D.

4-70. The key function at P1-12 is strapped from the front panel KEY-OFF-VOX/PTT switch, and the receiver through coupler function at P1-7 is controlled by the SIMPLEX-DUPLEX (figure 7-12) on the audio control unit. The receiver mute function at P1-C is extended through the backplane to transmit control head rear panel interface connector A7A10J1 but is not used. However, this line is also tied to J1-28 on the matrix card and receives inputs from the XMIT PWR switch on the transmit control head front panel. The servo function at P1-11 is also routed through the backplane to transmit control head rear panel interface connector A7A10J1 but is not used. When ground is applied or removed at any of these inputs, corresponding bits of the logic level monitor words (table 4-1 and 4-2) are set at logic 0 or logic 1 and the mode initiate flip-flop is set. This action advises the computer that new mode information is available. All of these functions are performed in the same manner as that described for the simplex and VOX functions in paragraph 4-69.

4-71. The frequency initiate input at P1-9 originates on the logic level slave card. A flip-flop similar to the mode initiate flip-flop (gates A12A and A11B) applies a logic 0 or logic 1 at P1-9 to control the condition of bit 4 of logic level monitor word 3 (tables 4-1 and 4-2). When the frequency initiate flip-flop on the logic level slave card is set, a logic 1 is present at P1-9. This signal is inverted by gate A13C and a logic 0 is applied to pin 5 of shift register A7, advising the computer that a new tune cycle is to be initiated.

4-72. Data loaded into the six 4-bit shift registers is read out serially to form the 24 data bits of the monitor words. This serial readout is enabled when the monitor clock, monitor gate 1, monitor gate 2, and monitor strobe signals at P1-H, P1-8, P1-J, and P1-6 are applied to pins 6, 7, and 8 of the shift registers. The monitor clock signal is a symmetrical square-wave signal generated by processor card A7A4 and buffered on the logic level slave card. (figure 4-1). The monitor gate and the monitor strobe inputs are generated on the logic level slave card and are described in succeeding paragraphs. When triggered by these timing signals, the data in the shift registers is serialized by readout from pin 9 to pin 1 of the preceding register. The registers are connected in A2, A7, A8, A4, A6, and A3 order. Bits in the registers are numbered sequentially from 0 through 23 with the first bit of each register corresponding to pin 5 and succeeding bits in pin 3, 2, 14 order. This arrangement establishes bit 0 at pin 5 of register A2, bit 11 at pin 14 of register A8, and bit 23 at pin 14 of register A3.

The serial output at pin 9 of register A2 therefore contains bits 0 through 23 that are inverted by gate A16D and applied to P1-K as monitor data.

4-73. BACKPLANE CONNECTIONS

4-74. The transmit and receive control head backplane cards, shown as blocks A7A8 and A8A3 in figure 4-1 have no functional circuits. The cards contain printed circuit tracks that make the required connections between the matrix cards, the logic level slave cards, the five circuit cards that make up the computer, and the rear panels of the control heads. Figure 7-4 shows the from/to connections made by the circuit tracks of the backplane card. The connections are listed alphabetically by function to facilitate ease in circuit tracing. Identical backplane cards are used in both the transmit and receive control heads. However, the backplane card used in the receive control head has external strapping between pins 69 and 71 of spaces A2, A5, A6, and rear interface connector J1. This strapping is required to complete the 5-volt dc bus normally completed on the circuit cards in the transmit control head.

4-75. LOGIC LEVEL SLAVE CIRCUITS.

4-76. The transmit and receive control head logic level slave cards, shown as blocks A7A1 and A8A1 in figure 4-1 are represented schematically by figure 7-5. Identical logic level slave cards are used in both control heads.

4-77. POWER INTERRUPT CIRCUIT. The power interrupt circuit of the logic level slave card consists of a logic driver made up of transistors Q3, Q4, Q5, associated components, and power interrupt flip-flop A18A/A18B. This circuit also functions in conjunction with frequency change/power interrupt flip-flop A7D/A13B and initiate indicator flip-flop A12D/A13A. In addition, the circuit controls the reset function of associated circuits.

4-78. Pin P1-72 of the logic level slave card is normally connected to the 5-volt dc bus. When this power is removed or interrupted, a logic 0 is applied to the base of transistor Q4, activating the power interrupt logic driver circuit (figure 7-5). As Q4 starts to conduct, C11 charges and during this interval a logic 0 is applied to pin 1 of A18A causing power interrupt flip-flop A18A/A18B to set. This action applies a logic 1 to P1-37 and controls the condition of bit 3 in logic level monitor word 3 (tables 4-1 and 4-2). At the same time a logic 0 is applied to pin 7 of A13B causing frequency change/power interrupt flip-flop A7D/A13B to reset. The resulting logic 0 output is gated through A14B and is then applied to lamp drivers A5B and A5C that provide a ground return path at P1-43. This ground return is extended to the control head front panel to light the INITIATE indicator (figures FO-2 and FO-3). The output of transistor Q5 is gated through A17B and A17C and holds power change flip-flop A10A/A10B and frequency initiate flip-flop A18C/A18D in a reset condition during the brief undefined interval after power is applied but before it has been detected. This logic 0 is also applied to P1-28 as an initiate reset for the mode initiate flip-flop on the matrix circuit card. At each power interruption, all of these flip-flops are reset to ensure proper operating condition when power is restored. When the 5 volts dc is restored at P1-72, power interrupt flip-flop A18A/A18B is reset by a monitor word 3 enable applied to P1-23. This logic 0 is produced by one-of-sixteen decoder A1 and is strapped to P1-23 through address strapping connector J3 on the control head rear panel. The monitor word 3 enable is gated through A16D and A16C resulting as a logic 0 input at pin 7 of A18B and P1-33.

4-79. FREQUENCY CHANGE CIRCUIT. The frequency change circuit consists of frequency change/power interrupt flip-flop A7D/A13B, initiate indicator flip-flop A18C/A18D, and associated gates and components.

4-80. When any of the FREQUENCY-MHz thumbwheel switches on the control head front panels are repositioned, a logic 0 is applied to P1-39 of the logic level slave card. This logic 0 resets frequency change/power interrupt flip-flop A7D/A13B. Because initiate indicator flip-flop A12D/A13A is set, logic 0 is applied to pins 5 and 6 of gate A14B and is extended to lamp drivers A5C and A5B. The lamp drivers then provide a ground path for the INITIATE indicator through P1-43. When the frequency INITIATE switch on the control head front panel is pressed, logic 0 is applied to P1-41 of the logic level slave card. The momentary logic 0 resets initiate indicator flip-flop A12D/A13A, and sets frequency change/power interrupt flip-flop A7D/A13B and frequency initiate flip-flop A18C/A18D. A logic 1 is now applied to pins 5 and 6 of AND gate A14B. The logic 1 output inhibits lamp drivers A5C and A5B causing the INITIATE

indicator on the front panel to go out. At the same time, the logic 0 is inverted by A18D and applied to P1-33. This output controls the condition of bit 3 of logic level monitor word 3 (tables 4-1 and 4-2). The on/off operation of the INITIATE indicator is also controlled by bit 30 of the logic level control word (table 4-3). This bit is received at pin 12 of shift register A6 and gated through A12A and A12B to set initiate indicator flip-flop A12D/A13A. The same bit controls reset of the flip-flop and is applied to pin 2 of A13A through gate A12C. The INITIATE indicator is also enabled when the XMIT PWR switch on the transmit control head momentarily removes ground from P1-35. The resulting logic 0 at pin 8 of A13B enables the circuit as described above.

4-81. MONITOR BUS DRIVER CIRCUITS. The monitor bus driver circuits consist of transistors Q1 and Q2, gates A8B, A15A, A15B, A15C, A15D, A14C, A14D, A16A, A16B, and associated components.

4-82. Serial data in the form of a 24-bit monitor word is received at P1-34 as MON DATA. This serial data is received from the matrix cards (figures 4-1 and 7-3) through the backplane card connections. The data is processed through the monitor bus drivers by the application of the monitor gate, the input/output gate and the monitor word enable output of gate A2. The waveform diagram on figure 7-5 illustrates how the monitor gate originating at flip-flop A3B inhibits A8B during the transmission of the 7-bit address field and the input/output bit. When the inverted input/output bit at pin 12 of A3A and the monitor gate at pin 8 of A8B become a logic 1, the MON DATA is gated to the respective monitor bus drivers and applied as true and false outputs at P1-48 and P1-46. These amplified outputs are routed through the backplane card and applied to the accessible memory card of the rom computer (figure 4-1).

4-83. LOGIC LEVEL CONTROL BUS CIRCUIT. Inputs for the logic level control bus circuit are the logic level clock, the logic level control bus, and the sync (LL DELIM). Each of these inputs are applied to the logic level slave card as true and false functions at pins 38, 44, 42, 40, 30, and 20 of P1 on logic level slave card (figure 7-5). All six inputs are applied to dual differential line receivers A20 and A19. These differential line receivers accept the true and false inputs and provide a single false output for each of the dual inputs.

4-84. The waveform table in figure 7-5 illustrates the condition of the sync (LL DELIM) input. As this synchronizing signal leaves pin 2 of A20, it is in an inverted (false) state. This $\overline{\text{sync}}$ signal is applied directly to pin 6 of shift registers A22 and A26 and is used as shift register mode control. A second branch of the $\overline{\text{sync}}$ is inverted by gate A21B and is applied to pins 2 and 6 of dual J-K masterslave flip-flop A3. Each time the sync signal falls to logic 0, J-K flip-flops A3A and A3B are reset. Data received on the logic level control bus is also in an inverted form at the output of differential line receiver A20. This serial data is applied in the false state to the J input (pin 14) of A3A and to pin 1 of 4-bit shift register A6. At the same time the control data is inverted by gate A21A and applied to the K input (pin 3) of A3A and to pin 1 of 4-bit shift register A22. The first seven bits of the control word data contains address information assigned by the computer program, but bit 1 of the address is not decoded by the logic level slave card. These bits are clocked into shift registers A22 and A26. When the sync signal is low, pin 13 of A22 is set to a logic 0, and all other outputs of registers A22 and A26 are set to logic 1. After the seven bits of the address are clocked into shift registers A22 and A26, the logic 0 at pin 13 of A22 has shifted to pin 9 of A26 and is fed back through A4C to inhibit further clock signals into A22 and A26. This signal is also inverted by A4B and provides one of the enables for one-shot multivibrator A8A and C1. Another enable signal is applied from pin 8 of A3B. On the next negative transition of the clock signal, the A3B enable goes low and remains low until the sync (LL DELIM) goes low. This enable signal prevents more than one strobe pulse on the MON STROBE line at P1-27. The third enable for the one-shot multivibrator is the logic level clock signal from pin 14 of A4D. Therefore, when the seven bits of the address are locked in registers A22 and A26 and when the logic level clock pulse goes positive, the MON STROBE applied to P1-27 goes high for approximately one microsecond and then falls to logic 0. (See waveform chart on figure 7-5). The high to low transition on the monitor strobe line samples the input/output bit into J-K flip-flop A3A. If the input/output bit is a logic 1, pin 13 of flip-flop A3A enables A2B so that control data can be stored in shift

registers A6 and A11. The output of pin 9 of A3B defines the transfer period for either monitor data or control data. This transfer occurs when the output of pin 9 goes to logic 1. When the input/output bit is logic 0, pin 12 of flip-flop A3A enables the monitor bus drivers through A8B. It should be noted that the monitor strobe pulse applied to P1-27 is extended to the matrix card where monitor data is strobed regardless of the condition (logic 1 or 0) of the input/output bit.

4-85. When the input/output bit is logic 1, the data on the logic level control bus is in the control word format shown in table 4-3. This data is clocked into registers A6 and A11 through pin 1 of A6. The data is in an inverted (false state). The data bits are clocked through the registers in serial form until the last bit (bit 31) enters the register. At this time, the sync signal falls to logic 0 and resets J-K flip-flops A3A and A3B. This action stops the serial data input to shift registers A6 and A11, leaving bits 24 through 31 of the logic level control word (table 4-3) set in the registers and available at the parallel outputs. These bits activate lamp drivers A5, A9, and A14B that light or turn off the control head front panel indicators shown in figure 7-5.

4-86. The lamp test 1 and lamp test 2 functions at pins P1-52 and P1-54 are strapped together at connector J1 of the control head rear panel and the common line is connected to the LAMP TEST switch on the respective control head front panels. When the LAMP TEST switch is pressed, ground is applied to both lamp test inputs of the logic level slave card and the lamp drivers provide ground return paths for all the front panel indicators, regardless of the condition of the bits in shift registers A6 and A11.

4-87. The monitor gate derived at the Q output of J-K flip-flop A3B is inverted by gates A7A and A7B that provide two outputs to pins P1-31 and P1-32. The $\overline{\text{monitor gate 1}}$ and $\overline{\text{monitor gate 2}}$ outputs are routed to the matrix card where they are used as a mode control input to the six 4-bit shift registers that store the monitor word data.

4-88. ONE-OF-SIXTEEN DECODER CIRCUIT. One-of-sixteen decoder A1 provides the three monitor word enable and the one control word enable signal required for the transmit and receive control heads to function. Because pin P1-64 of the logic level slave card is strapped to ground through the backplane card and rear panel connector J1 on the respective control heads, pins 18 and 19 of decoder A1 are held at a constant logic 0. The remaining inputs at pins 20, 21, 22, and 23 are controlled by the computer program and are applied as parallel outputs of shift registers A22 and A26. The data in these registers consists of the first seven (address) bits of the logic level control word (table 4-3). The sixteen address decode (adrs dcd) outputs of decoder A1 are routed through the backplane card to address strapping connector J3 on the rear panel of the transmit and receive control heads (figure 4-1). At these connectors, the address decode functions that are used are looped back through the backplane card to pins 23, 25, 26, and 60 of connector P1 on the logic level slave card. Four different address decode outputs are used in each control head. The following listing shows the binary inputs required at pins 20, 21, 22, and 23 of decoder A1 to produce the logic 0 outputs on the address decode lines.

INPUTS					
PIN A1-23	PIN A1-22	PIN A1-21	PIN A1-20	ADRS DCD NUMBER	FUNCTION
0	1	1	1	15	Xmt mon word 1 enable
0	1	1	0	7	Xmt mon word 2 enable
0	1	0	1	11	Xmt mon word 3 enable
1	0	0	0	2	Xmt control word enable
0	0	1	0	5	Rcv mon word 1 enable

INPUTS					
PIN A1-23	PIN A1-22	PIN A1-21	PIN A1-20	ADRS DCD NUMBER	FUNCTION
1	0	0	1	13	Rcv mon word 2 enable
0	0	0	1	9	Rcv mon word 3 enable
0	1	0	0	3	Rcv control word enable

4-89. Use of the one-in-sixteen decoder enables the computer to request frequency and mode information from the transmit and receive control heads by inserting the required logic in the address field of the logic level control words (table 4-3). This address data is then decoded by decoder A1 and a logic 0 is produced on the appropriate address decode line. The logic 0 is then strapped back to the monitor and control word enable inputs of the logic level slave card to activate the circuits previously described. The monitor word enable signals applied to pins P1-23, P1-25, and P1-26 of the logic level slave card are also wired to the control head front panel inputs shown in figures 7-1 and 7-2. The computer also transmits receiver and transmitter operational status in the control word. The enable for the logic level control word is applied by decoder A1 to pin P1-60 of the logic level slave card through the rear panel strapping connector. Gate A25A inverts the logic 0 and applies a logic 1 to A2B to permit the control word to be clocked into shift registers A6 and A11. Gate A7C also routes the control word enable to the set and reset inputs of initiate indicator flip-flop A12D/A13A.

4-90. ROM COMPUTER CIRCUITS.

4-91. GENERAL. The rom computer consists of hardwire memory card A7A2, CCCS timing card A7A3, processor card A7A4, instruction decode card A7A5, and accessible memory card A7A6. These cards are in the transmit control head as indicated in figure 4-1. All the inputs and outputs of the computer are made via the logic level and CCCS buses, using the accessible memory card as the interface. Interconnections between the five circuit cards that make up the computer, as well as connections with other circuits of the radio control group, are made through backplane card A7A8. For this reason, close reference to the backplane card schematic diagram (figure 7-4) aids in understanding the description of the individual circuit cards that are presented in the following paragraphs. Many of the functions at the input and output pins of the computer circuit cards are shown as mnemonics on the detailed logic diagrams referenced in the description. For clarity, these mnemonics are defined the first time they are used and a complete alphabetical listing of the mnemonics and their meaning is included in the glossary of the introduction to this manual.

4-92. ACCESSIBLE MEMORY CIRCUITS. Accessible memory card A7A6 contains the input/output circuits for the rom computer. Figure 7-6 is a detailed logic diagram that illustrates the functions of these circuits.

4-93. Logic Level Clock Bus Driver. The CLL (clock, logic level) applied to pin P1-35 of the accessible memory card is a 256-kHz symmetrical square-wave timing signal. This signal is generated on processor card A7A4, is applied to inverter/line drivers A18C and A18B, and produces the LL (logic level) clock and $\overline{\text{LL clock}}$ outputs at pins P1-38 and P1-36. These two functions are then routed through backplane card A7A8 to pins 38 and 44 of the logic level slave card (figure 7-5). Refer to figure 4-2 for characteristics of the logic level clock bus signal.

4-94. Logic Level Sync (Delimiter Bus) Driver. The IDRT (processor time interval signal) applied to P1-10 of the accessible memory card also originates on processor card A7A4. This signal is routed through inverter/line driver A12D and gate A26D to inverter/line drivers A18F and A18E. The resulting sync and $\overline{\text{sync}}$

outputs at P1-30 and P1-20 are then routed through the backplane card and applied to pins 30 and 20 of the logic level slave card. This synchronizing signal output is the logic level delimiter bus illustrated in figure 4-2. Because the YN (logic level sync enable) signal at P1-26 is also gated through A26D the output of A26D applied to A18F is the inverted result of a normal AND function. The YN input at P1-26 is received from instruction decode card A7A5 when the program selects data to be transmitted or received on the logic level bus.

4-95. Logic Level Monitor Circuit. The $\overline{\text{LL}}$ monitor bus and the LL monitor bus inputs at pins 46 and 48 of the accessible memory card are received from the logic level slave cards (figure 7-5). These inputs are the true and false states of the 24-bit monitor words formed by the serial outputs of the shift registers on the matrix cards. Differential line receiver A23A on the accessible memory card accepts the two inputs and provides the SWO (logic level input bus) at P1-47. The SWO signal is the LL monitor bus (figure 4-2) and is applied to the accessible memory data selector circuit of instruction decode card A7A5 (figure 7-7). When the computer program requests this data, the SWO data is converted to DBI (data bank input) and is applied to pin P1-7 of the accessible memory card (figure 7-6).

4-96. Accessible Memory Data Bank. The accessible memory data bank consists of dual 32-bit static registers A4, A10, A16, A17, A22, A28, A29, and A31. The dual configuration provides 16 registers each capable of storing 32 bits of information. Access to each register is made independently by program control. Serial data inputs to the registers are received via the DBI line at P1-7 on the accessible memory card. The data is changed from transistor to transistor logic (TTL) to metal oxide semiconductor (MOS) logic by interface converter A2B and applied to the registers along a common line. Two 8-channel multiplex switches (A9 and A27) function as a demultiplexer. These switches apply clock to the specific registers selected by the four AL (monitor storage address) inputs at P1-15, 16, 17, and 18 or the A, B, C, and D (accessible memory address) inputs at P1-11, 12, 13, and 14. As clock is applied to the selected registers, the information on the DBI line is clocked into the registers. The A, B, C, and D inputs are the first of four bits of the program instructions received from the instruction memory circuits of instruction decode card A7A5. Inputs AL1 through AL4 define the first storage location of the CCCS bus monitor words (figure 4-3). Both groups of address information are weighted 8, 4, 2, 1 so that registers 0 through 15 of the data bank can be selected to store the DBI information. It should be noted that register 0 is the accumulator that is part of hardwire memory card A7A2. The accumulator is accessed when four 0's are present at the A, B, C, D, or AL1, AL2, AL3, AL4 inputs (during a CCCS input cycle) and an S1 (accumulator output) signal is applied to P1-9 and gate A26A. The IDS (input CCCS data signal) at P1-65 determines which set of register address inputs directs clock to demultiplexer A9 and A27 to select the registers that store the DBI. The IDS signal originates at the input/output timing generator on CCCS timing card A7A3.

4-97. Multiplexers A15 and A30 accept the parallel outputs of the selected data bank registers and produce a serial output that is applied to level converter A21A and inverter A12C. Gates A25D and A25B select between the multiplexer output and the accumulator output to provide the DBO (data bank output) data. This data goes to pin P1-45 and is also routed through the logic level address select gates to pins P1-40 and P1-42. This second output is the logic level control bus and is routed through the backplane card to the logic level slave card as separate true and false functions. In order for the DBO to be gated to the logic level control bus outputs, the program enables the following conditions.

a. An EEL (logic level address enable) signal from processor card A7A4 must be applied to P1-44 and gates A24A and A24C.

b. An LLA (logic level address) signal from the logic level address selector on instruction decode card A7A5 must be applied to P1-43 and gate A24B.

c. A YN (logic level sync enable) signal from instruction decode card A7A5 must be applied to P1-26 and gates A24B, A24A, and A26D.

4-98. Register 16 of the data bank is reserved for receipt of nonsynchronous fault data and does not receive its input from the DBI line. FI (fault data in) at P1-27 is applied to register 16 via interface converter A3A and pin 1 of dual

32-bit register A22. This FI input and the FIC (fault data clock) at P1-31 are received from the CCCS bus fault detector circuit of CCCS timing card A7A3. The fault data is clocked into data bank register 16 by the FIC when the computer is in a CCCS output cycle. The fault data is shifted to another register by a program instruction that enables the STR-F (store fault data) at P1-32. When P1-32 is enabled the fault data is routed from FD (fault register output) P1-5 through the instruction decode card A7A5 and appears as DBI input at P1-7. Dual J-K flip-flops A8 and A14 use the Ø3 (phase 3 clock signal) P1-37 for timing to sequence the fault data during the CCCS output cycle. The FL (CCCS fault inhibit) at P1-29 prevents fault data from being stored until a final verification is made on CCCS timing card A7A3.

4-99. Radio Counter Address Driver Circuit. The strap 1 and strap 2 functions at P1-23 and P1-24 of the accessible memory card are extended through the backplane and the rear panel wiring (table 7-5) to connector A7A10J3. In this configuration, no further connections are made at connector A7A10J3. Therefore, a logic 1 is constantly applied to pin 2 of gate A11A and pin 12 of gate A11D, permitting the CA (radio counter state A) at P1-28 and the CB (radio counter state B) at P1-19 to control the CRA (radio counter address bit 1) and CRB (radio counter address bit 2) outputs. The CA and CB inputs originate at the radio group counter on instruction decode card A7A5, and the CRA and CRB outputs are routed back to the instruction decode card and are applied to the logic level address selector circuit.

4-100. Control Bus Circuit. The control data applied at pin P1-51 of the accessible memory card consists of logic level 32-bit words, 24 bits of which are the monitor data shown in tables 4-1 and 4-2 and the remaining 8 bits are the 7-bit address field and the input/output bit illustrated in figure 4-2. The data words are applied to thin film modulator A33 where the data is biphase modulated on a 4800-Hz carrier generated by thin film oscillator A34. True and false outputs are available at P1-52 and P1-50. These outputs are applied to the CCCS bus that connects the radio control group and the radio equipment DCU's (figure 4-1).

4-101. Monitor Bus Circuits. CCCS bus monitor words (figure 4-3) are received from the radio equipment DCU's in the true and false state at P1-66 and P1-64 of the accessible memory card. These 32-bit biphase modulated monitor words are demodulated to logic level form by thin film demodulator A32. The demodulated (logic level) output is applied to P1-63 as monitor data and is further extended to CCCS timing card A7A3. The monitor gate at P1-57, the CCCS clock at P1-61, and the TCSC (CCCS timing input) at P1-59 are outputs of oscillator A34 and demodulator A32. These functions are applied to the CCCS bus fault detector circuit of CCCS timing card A7A3.

4-102. Carrier Bus Circuit. The carrier bus and $\overline{\text{carrier bus}}$ outputs at P1-56 and P1-58 of the accessible memory card is the 4800-Hz carrier bus extended to the radio equipment DCU's. This carrier is illustrated in figure 4-3 and the routing through the radio control group is shown in figure 4-1.

4-103. INSTRUCTION DECODE CIRCUITS. Instruction decode card A7A5 stores and decodes instructions and data received from hardwire memory card and routes data to and from accessible memory according to the program instructions being processed. The following circuit descriptions are keyed to the detailed logic diagram included in figure 7-7.

4-104. Instruction Memory Circuit. The instruction memory circuit consists of 4-bit serial shift registers A12, A8, A6 and A7. This memory circuit has two basic inputs: the INC (instruction storage clock) applied to P1-29 and the MDO (memory data output) applied to P1-23. The INC signal originates on processor timing card A7A4 and consists of a burst of 32 pulses during the instruction read cycle. The MDO input contains instruction words or process parameters from hardwire memory card A7A2. During the instruction read frame, the MDO line always contains instruction data that is read into the instruction memory registers. During the process frame, the MDO line may contain parameter data to be used by either the operator or branch circuits; otherwise it contains instruction data to be read during the next read frame. The instruction read during the previous read frame determines how this second word of MDO data is interpreted. There are two types of parameter data: branch address parameter data (discussed below) and operator parameter data. The entry point for operator parameter data is A28D. These operator gates compare the MDO data field with

an accessible memory field during logical operations. Because the process frame is never coincident with the instruction read frame, parameter data is never read into the instruction memory registers. If the instruction was a conditional branch and if the branch test was positive, then an extra computer frame is inserted between the process frame and the program advance frame called the branch load frame. During the branch load frame, MDO data (branch address) is enabled at accumulator data select gate A18A and inverted MDO data is applied to $\overline{ACD}$ output at P1-35. The signal on $\overline{BR}$ at P1-3 is low during this interval. During the instruction read frame, the MDO data is 16 bits wide. These 16 bits are scanned twice and the data read from the MDO during the first 16 bits is compared with the data read during the second 16 bit interval. If the data does not compare, the program is reinitiated at step zero. If the data does compare, the 16-bit MDO instruction is left in the registers A12, A8, A6, and A7 and the process frame begins. Parameter data has no validity check. The process frame is also 32 bits wide. The 16 bits of MDO operator parameter data can fill either the first or second half of the process frame and the remaining 16 bits are specified to be either all 1 or 0 as determined by the instruction. MDO branch address parameter data is scanned into the accumulator twice during the branch load frame. This dual scanning causes the first 16 bits in the accumulator to be identical to the second 16 bits. The first four bits of the instruction word are parallel outputs of register A7 and provide the A, B, C, and D outputs at P1-12, 11, 14, and 13. These weighted outputs are applied to accessible memory card A7A6 (figure 7-6) where they select data bank registers 1 through 15 to be accessed during the process frame. When the output of register A7 is 0-0-0-0, the accumulator on hardwire memory card A7A2 is accessed. Bits 5 through 9 of the instruction word are the four parallel outputs of register A6 with bit 9 coming from pin 6 of register A8. Combinations of these five bits, are applied to 8-input multiplexer A11, dual 4-bit comparator A15, gates of the operator section, radio group counter A2, and to the AL1 through AL4 (monitor storage address) outputs at P1-15 through P1-18. When 8-input multiplexer A11 is sequenced by the $\overline{WT1}$, $\overline{WT2}$, and $\overline{WT4}$ inputs at P1-51, P1-52, and P1-53, the LLA is read out serially at P1-44. This LLA output consists of eight bits. The first five bits are bits 5 through 9 of the instruction word that are applied to pins 1 through 5 of multiplexer A11. The next two bits are the CRA and CRB applied to P1-21 and P1-22. Bit 8 is the input/output bit applied to pin 9 of A11 by one-of-sixteen decoder A13. Figure 4-2 shows the relationship of this 7-bit address field and the input/output bit. The LLA is then routed to accessible memory card A7A6 where it is processed with DBO on the logic level control bus. This address is transmitted only during the process frame of a logic level output/input instruction.

4-105. The instruction data in register A6 may also define the address of the data bank register that receives CCCS bus monitor data. In this instance, the four bits in register A6 are routed through P1-16, 15, 18, and 17 to accessible memory card A7A6 where they select the address of the data bank register which will receive the first monitor response during a CCCS output/input sequence. Bits 5 through 9 of the instruction word are also routed to gates A28, A24, and A1 of the operator section where they enable circuits to perform logical AND, OR, ADD, and exclusive OR operations on the data selected by the programmed instructions.

4-106. Bit select instructions use comparator circuit A15. Any bit (0 through 31) of the process frame can be determined from $\overline{WT1}$ through $\overline{WT16}$ inputs at P1-51, 52, 53, 55 and 57. During the bit interval selected by bits 5 through 9 of the instruction word, the output of A15 goes high. This signal is used by the operator circuits during bit select instructions to select the OPO (operator output) at P1-59. The output of dual 4-bit comparator A15 is also used during the rotate instruction to inhibit the processor clock during the process frame. This inhibit capability allows a programmable shift in the data fields of the data bank registers. The inhibit is activated when the $\overline{ROT-E}$ output at P1-27 goes low.

4-107. Bit 10 of the instruction word is the EMB (accumulator clock enable) bit. This bit is read out of pin 8 of shift register A8 and is applied to processor card A7A4 through P1-31 to enable or inhibit the accumulator clock. Bit 11 of the instruction word is read out of shift register A8 at pin 11. This bit is applied to A18D and A4D to enable selected data to be loaded into the accumulator or routed through the operator section to the OPO at P1-59. Bit 12 of the instruction word is readout of register A8 at

pin 13. This bit is applied to A23C, A9B, and A4C. The bit enables gates that permit selected input data to be routed to the DBI output at P1-8, or to the $\overline{ACD}$ (accumulator input bar) at P1-35, or to the OPO output at P1-59.

4-108. Instruction Decode Circuit. The instruction decode circuit consists primarily of one-of-sixteen decoder A13 and gates A4, A5, A9, A14, A16B, A16C, A17A, and A17B. When a reset logic 0 is applied to P1-07, decoder A13 is inhibited by the logic 1 applied to pin 19. As this potential is changed to logic 0, bits 13 through 16 of the instruction word are applied to pins 23, 22, 21, and 20 to control the output of the decoder. The binary equivalent of these four bits of the instruction word causes one of the outputs at pins 1 through 11 and 13 through 17 to produce a logic 0 output. Only one output can be logic 0 at a time, and all other outputs remain logic 1 until a new instruction is received on the MDO and read into the instruction memory shift registers. Following is a short summary of the functions enabled as decoder A13 outputs logic 0 at each of the 16 output pins. This summary is not intended to be an explanation of all the logic functions performed by the operator section of the instruction decode card but aids in understanding the overall operation and in isolating faults.

a. Pin 1 provides the input/output bit to pin 9 of 8-input multiplexer A11, applies a logic 1 on the YN line at P1-26, and enables A22D that allows the SWO to be gated to the ACD.

b. Pin 2 applies a logic 1 on the YN line at P1-26.

c. Pin 3 applies a logic 1 on the OUTS (output sine wave) line at P1-47, enables gates A22A and A23D permitting the monitor data at P1-64 to be gated to the DBI or $\overline{ACD}$ outputs, and enables A14D and A18A allowing parameters on the MDO input to be clocked into the accumulator through the ACD output at P1-35.

d. Pin 4 enables A9B or A4B depending upon the condition (logic 1 or 0) of bit 12 of the instruction word (pin 13 of register A8). When A4B is enabled, the output of A4A enables A22C and allows the S1 at P1-9 to be clocked to the DBI or $\overline{ACD}$ outputs. When A9B is enabled, the S1 input is gated through A25D to replace the MDO operator parameter for selected logic instructions.

e. Pin 5 applies a logic 1 on the STR-F output at P1-32 and enables A22B so that the FD (fault register output) at P1-6 can be gated to the DBI output at P1-8 or P1-35.

f. Pin 6 applies a logic 1 on the COZ + BNZ + CNZ (branch signal) output at P1-19 and enables A27B, A28B, allowing the operator section to act upon inputs from the DBO at P1-46 and the output of dual 4-bit comparator A15. This is a selected bit branch test such that a branch load frame is initiated if the selected bit is zero.

g. Pin 7 applies a logic 1 on the COZ + BNZ + CNZ output at P1-19 and enables A28B allowing the output of dual 4-bit comparator to be gated through the operator section. This is a selected bit branch test such that a branch load frame is initiated if the selected bit is one.

h. Pin 8 applies a logic 1 on the COZ + BNZ + CNZ output at P1-19 and enables A30A. This is a conditional branch test such that a branch load frame is initiated if any bit in the field is one.

i. Pin 9 applies a logic 0 on the BPZ (branch indirect bar) output at P1-41.

j. Pin 10 enables A23B that permits parameter data to be clocked to the DBI or ACD outputs, applies a logic 1 on the LCD (literal code signal) output at P1-25, enables A28D and A28A allowing the operator section to process the data to the OPO.

k. Pin 11 enables A3B and A3C and permits clock to be applied to dual J-K flip-flop A2 that functions as the radio group counter.

l. Pin 13 applies a logic 1 on the LCD output at P1-25, enables A18B that allows the OPO to be gated to the DBI or ACD, enables A1A, A1B and A1D allowing bits 7, 8, and 9 of the instruction word to select either AND, exclusive OR, or logical OR functions in the operator section.

m. Pin 14 enables A23A allowing the OPO to be clocked to the DBI or ACD, enables A28C allowing the output of dual 4-bit comparator A15 to be gated through the operator section, and enables A30C selecting an AND operation. This allows a selected bit in the DBI data field to be set unconditionally to zero.

n. Pin 15 enables A23A allowing the OPO to be gated to the DBI or ACD, enables A30A selecting a logical OR operation, and enables A28B that allows the output of dual 4-bit comparator A15 to be gated through the operator section. This allows a selected bit in the DBI data field to be set unconditionally to one.

o. Pin 16 enables A26C and permits the ROTE (rotate enable) to be applied to P1-27.

p. Pin 17 enables A30B and permits the sum output at pin 5 of adder A31 to be gated to the OPO, applies a logic 1 on the LCD output at P1-25, enables A18B allowing the OPO to be clocked to the DBI or ACD, enables A28D and A28A allowing data to be clocked into adder A31.

4-109. Operator Section Circuits. The operator section of instruction decode card A7A5 consists primarily of 4-wide 3-2-2-3 input AND-OR-invert gates A18, A22, A23, A28, and A30, adder A31, dual 4-bit comparator A15, and associated gates. These components perform AND, exclusive OR, logical OR, or AND functions on the data selected by instruction words received from hardwire memory card A7A2. The fundamental operations of the operator section are controlled by bits 5 through 9 of the instruction words as listed below.

a. Bit 5 determines whether all 1's or all 0's fill the unspecified portion of the operator parameter word.

b. Bit 6 determines whether the operator parameter data occurs in the first or second half of the process cycle.

c. Bit 7 controls the AND function performed by A30D and associated inputs.

d. Bit 8 controls the logical OR function performed by A30A and associated inputs.

e. Bit 9 controls the exclusive OR function performed by adder A31 and gate A30B.

4-110. Radio Group Counter Circuit. The radio group counter of instruction decode card A7A5 consists of dual J-K flip-flops A2 and gates A3A, A3B, and A3C. The external strap at P1-24 is grounded at connector A7A10J3 on the rear panel of the transmit control head. The flip-flops are reset when bit 7 of the instruction word from pin 11 of register A6 is at logic 1 and decoder A13 applies a logic 0 to A21C. This counter is incremented by program instruction. The CA output at P1-28 and CB output at P1-20 sequence once per instruction as follows: (1,0), (0,1), (1,1) and (0,0) until the next reset instruction occurs changing the CA and CB outputs to logic 0. The CA and CB functions are routed to accessible memory card A7A6 (figure 7-6) where they are gated through the radio counter address driver circuit that supplies the CRA and the CRB inputs at pins P1-21 and P1-22 of the instruction decode card.

4-111. HARDWIRE MEMORY CIRCUITS. Hardwire memory card A7A2 contains the program that controls the overall activity of the radio control group. The card includes program storage circuits, an instruction address counter, an accumulator, and a read verifier. There are two physically different hardwire memory cards used in the radio control group. Early models of the radio control group use card 789-2620-001 and later models use card 633-9332-001. The form, fit, and function of these two cards are identical and they can be used in any model of the radio control group. Because the internal functions of these cards are slightly different, the functions of both cards are included. Paragraphs 4-112 through 4-116 describe card 789-2620-001 and paragraphs 4-116A through E describe card 633-9332-001. Refer to figures 7-8 and 7-8A for detailed logic diagrams of the two cards.

4-112. Program Storage Circuits (Card 789-2620-001). Memory modules A1, A2, A3, A5, A6, and A7 contain 768 16-bit instruction words. These instruction words include a capability for performing logic operations and initiating the transmission of control and monitor data on the CCCS and logic level buses. Logical operations include AND, exclusive OR, and logical OR operations between literal numbers and an accessible memory data bank register or between the accumulator and any accessible memory data bank register. Individual bits of the data in the accessible memory data bank registers can be modified to 1 or 0 or checked for the presence of 1 or 0 by the appropriate instructions in the hardwire memory modules. In addition, data fields within the memory can be further manipulated by using instructions that perform add or rotate functions. Other instructions control data transmissions on the CCCS bus, select the accessible memory

data bank register containing the data to be transmitted on the control bus, select the subaddress to be associated with the selected control data, designate the accessible memory data bank registers that receive the monitor words from the DCU's, and provide the information to generate DCU addresses that are transmitted with CCCS bus control words. The logic level bus is serviced by a separate set of instruction words. These instructions determine the logic level address for the logic level control words, whether a control word is transmitted or a logic level monitor word requested, and the address of the accessible memory data bank register that provides data for the logic level control word or storage for the requested monitor word.

4-113. The 16-bit instruction words are made up of 8 bits from memory modules A1, A2, A3 and a second group of 8 bits from memory modules A5, A6, and A7. The timing for the memory modules is provided by the Ø3 and the Ø1 signals applied to P1-37 and P1-65. The specific instruction word is selected by the instruction address counter outputs applied to the memory modules through level changers A18, A19, A24, A25, A30, and A31A. Instructions are read out of memory in sequential order starting with memory position 0 and progressing to the last instruction necessary to accomplish the required task. Exceptions to this sequence are the branch instructions that enable the program to skip to an instruction later in the sequence or return to a previous instruction and continue the sequence. As the instruction words are read out of memory, the data is parallel loaded into multiplex switches A4 and A14. The $\overline{WT8}$, $\overline{WT4}$, $\overline{WT2}$, and $\overline{WT1}$ timing signals then read the instruction words out of the multiplex switches in serial form. This serial output from pin 3 of A4 and A14 is applied to MDO driver Q1 that shapes and level-shifts the module data. Gates A13A, A13D and flip-flop A12 retime the data to prevent skew in later processing. The Ø3 applied to pin 3 of A12 clocks the instruction word out the Q output of A12 through inverter A11B to the MDO at pin P1-24. The $\overline{Q}$ output at pin 12 of A12 is applied to the read verifier circuit described below.

4-114. Read Verifier Circuit (Card 789-2620-001). The instruction words read out of the memory modules are 16 bits long and the read time interval is 32 bits long. Therefore, the instruction words are read twice. The MDO output at P1-24 is routed to instruction decode card A7A5 where the instruction word is clocked into the instruction memory registers (figure 7-7). Because the read time interval is 32 bits long, the instruction word leaves the instruction decode card at the D output and is routed back to hardwire memory card A7A2 at P1-14. The bits of the instruction word received on the D input are then compared with the $\overline{Q}$ output at pin 12 of flip-flop A12. The comparison is accomplished as the two inputs are clocked through gates A20A and A20B that are enabled by the $\overline{WT16}$ and reset timing signals applied to P1-58 and P1-8. If the two data fields compare, a logic 1 is applied to FINS (fault in instruction register) and the instruction word is processed. If the two data fields do not compare, a logic 0 is applied to the FINS output. This logic 0 is then applied to processor card A7A4 where a PI (power interrupt) signal is generated and applied to P1-15 of the hardwire memory card. This PI signal resets the instruction address counter to 0 and also resets J-K flip-flop A26.

4-115. Instruction Address Counter (Card 789-2620-001). The instruction address counter consists of hexadecimal counters A17, A23, and A29. These counters function as a single unit that determines the sequencing of the program steps. An IAC CLOCK (instruction address counter clock) pulse is applied to P1-64 at the end of every instruction read interval, and if the instruction requires two 16-bit words another IAC CLOCK pulse is generated at the end of the processing interval. When the program requires a break from sequential processing (a branch), the next instruction address (branch to address) is serially loaded into the accumulator during the third time interval of the processing cycle. After the new address is stored in the accumulator, an IAC load pulse is applied to P1-62 to store the address in the instruction counter.

4-116. Accumulator Circuit (Card 789-2620-001). The accumulator of hardwire memory card A7A2 consists of 8-bit shift registers A15 and A21 and 4-bit shift registers A16, A22, A28, and A27. Serial data from instruction decode card A7A5 is applied to P1-35 on hardwire memory card A7A2 as $\overline{ACD}$. The data is shifted into the 32-bit accumulator by the accumulator clock signal applied at P1-39. The serial data input and the clock are controlled by the instruction words from the memory modules. When the memory instructions select the CCCS input/output mode of operation (control words are sent to the radio equipment and monitor words are received from the DCU's via the CCCS bus), the accumulator is loaded

from the memory modules through the instruction decode card with DCU address information. This information is presented to the CCCS timing card through 10 parallel outputs: eight EA (address enable) outputs at P1-53, 47, 48, 44, 42, 40, 38, 36 and two CCCS subaddress 1 outputs (S1 and S2) at P1-10, and 6. These signals are static during the CCCS input/output mode. When the instruction words select any other mode of operation, the S1 output becomes the output of the accumulator and is routed back to the instruction decode card under program control.

4-116A. Program Storage Circuits (Card 633-9332-001). Memory modules U11 and U21 contain 1024 16-bit instruction words. These instruction words include a capability for performing logic operations and initiating the transmission of control and monitor data on the CCCS and logic level buses. Logical operations include AND, exclusive OR, and logical OR operations between literal numbers and an accessible memory data bank register or between the accumulator and any accessible memory data bank register. Individual bits of the data in the accessible memory data bank registers can be modified to 1 or 0 or checked for the presence of 1 or 0 by the appropriate instructions in the hardwire memory modules. In addition, data fields within the memory can be further manipulated by using instructions that perform add or rotate functions. Other instructions control data transmissions on the CCCS bus, select the accessible memory data bank register containing the data to be transmitted on the control bus, select the subaddress to be associated with the selected control data, designate the accessible memory data bank registers that receive the monitor words from the DCU's, and provide the information to generate DCU addresses that are transmitted with CCCS bus control words. The logic level bus is serviced by a separate set of instruction words. These instructions determine the logic level address for the logic level control words, whether a control word is transmitted or a logic level monitor word requested, and the address of the accessible memory data bank register that provides data for the logic level control word or storage for the requested monitor word.

4-116B. The 16-bit instruction words are made up of 8 bits from memory module U11 and a second group of 8 bits from memory module U21. The timing for the access operation is provided by the Ø3 and Ø1 signals applied to P1-37 and P1-65. The specific instruction word is selected by the instruction address counter outputs (figure 7-8A) that are applied to the memory modules. Instructions are read out of memory in sequential order starting with memory position 0 and progressing to the last instruction necessary to accomplish the required task. Exceptions to this sequence are the branch instructions that enable the program to skip to an instruction later in the sequence or return to a previous instruction and continue the sequence. As the instruction words are read out of memory, the data is parallel loaded into multiplex switch U31. The $\overline{WT8}$, $\overline{WT4}$, $\overline{WT2}$, and $\overline{WT1}$ timing signals then read the instruction words out of the multiplex switch in serial form. This serial output from pin 5 of U31 is applied to the J and K inputs of flip-flop U63A, which retimes the data to prevent skew in later processing. The Ø3 applied to pin 1 of U63A clocks the instruction word out the Q output of U63A through inverter U51 to the MDO at pin P1-24. The $\overline{Q}$ output at pin 14 of U63A is applied to the read verifier circuit described below.

4-116C. Read Verifier Circuit (Card 633-9332-001). The instruction words read out of the memory modules are 16 bits long and the read time interval is 32 bits long. Therefore, the instruction words are read twice. The MDO output at P1-24 is routed to instruction decode card A7A5 where the instruction word is clocked into the instruction memory registers (figure 7-7). Because the read time interval is 32 bits long, the instruction word leaves the instruction decode card at the D output and is routed back to hardwire memory card A7A2 at P1-14. The bits of the instruction word received on the D input are then compared with the $\overline{Q}$ output at pin 14 of flip-flop U63A. The comparison is accomplished as the two inputs are clocked through gates U61 and U62 that are enabled by the $\overline{WT16}$ and reset timing signals applied to P1-58 and P1-8. If the two data fields compare, a logic 1 is applied to FINS (fault in instruction register) and the instruction word is processed. If the two data fields do not compare, a logic 0 is applied to the FINS output. This logic 0 is then applied to processor card A7A4 where a PI (power interrupt) signal is generated and applied to P1-15 of the hardwire memory card. This PI signal resets the instruction address counter to 0 and also resets J-K flip-flop U63B.

4-116D. Instruction Address Counter (Card 633-9332-001). The instruction address counter consists of hexadecimal counters U12, U13, and U22. These counters function as a single unit

that determines the sequencing of the program steps. An IAC CLOCK (instruction address counter clock) is applied to P1-64 at the end of every instruction read interval. If the instruction requires two 16-bit words, another IAC CLOCK pulse is generated at the end of the processing interval. When the program requires a break from sequential processing (a branch), the next instruction address (branch to address) is serially loaded into the accumulator during the third time interval of the processing cycle. After the new address is stored in the accumulator, and IAC LOAD PULSE is applied to P1-62 to store the address in the instruction address counter. The IAC CLOCK and the IAC LOAD PULSE applied to P1-64 and P1-62 are retimed by a delay circuit consisting of J-K flip-flops U71A, U72A, and U72B. The retiming delays the rising edge of the pulses exactly one clock cycle to delay memory data output at P1-24 by one bit. This delay is necessary to ensure compatibility with processor timing.

4-116E. Accumulator Circuit (Card 633-9332-001). The accumulator of hardwire memory card A7A2 consists of 8-bit shift registers U42 and U52 and 4-bit shift registers U32, U33, U43, and U53. Serial data from instruction decode card A7A5 is applied to P1-35 on hardwire memory card A7A2 as $\overline{\overline{ACD}}$. The data is shifted into the 32-bit accumulator by the accumulator clock signal applied to P1-39. The serial data input and the clock are controlled by the instruction words from the memory modules. When the memory instructions select the CCCS input/output mode of operation (control words are sent to the radio equipment and monitor words are received from the DCU's via the CCCS bus), the accumulator is loaded from the memory modules through the instruction decode card with DCU address information. This information is presented to the CCCS timing card through 10 parallel outputs: eight EA (address enable) outputs at P1-53, 47, 48, 44, 42, 40, 38, 36 and two CCCS subaddress outputs (S1 and S2) at P1-10 and P1-6. These

signals are static during the CCCS input/output mode. When the instruction words select any other mode of operation, the S1 output becomes the output of the accumulator and is routed back to the instruction decode card under program control.

4-117. CCCS TIMING CIRCUITS. CCCS timing card A7A3 contains circuits that perform data link functions for the CCCS bus. These circuits function during the transmission of data to the DCU's on the control bus and during the reception of monitor data from the DCU's. The following description is keyed to the detailed logic diagram presented as figure 7-9.

4-118. The SDT (set for data transfer) input at P1-12 is the primary control for the operation of the CCCS timing card circuits. This input is a static logic 1 or logic 0 that originates on processor timing card A7A4 and is under program control. When a logic 0 is applied to the SDT input, idle words are transmitted on the CCCS bus. A logic 1 at this input sets flip-flop A15B and the resulting logic 1 at pin 9 of A15B sets flip-flop A15A and enables A29A and A33A. The enabled gates permits the TCSC (CCCS timing input) at pin P1-30 to be applied to pin P1-7 as the processor clock. This signal is a 4800-Hz square wave that is extended to processor timing card A7A4 where it provides the DBC (data bank clock) during the CCCS input/output data exchange period. J-K flip-flops A15A and A15B sequence the input/output intervals for the CCCS timing circuits.

4-119. CCCS Bus Transmit Functions. When the CCCS bus input/output functions are enabled by instruction words from hardwire memory card A7A2, EA1 through EA8 are applied to CCCS timing card A7A3. These enable signals are a combination of static logic 1 and 0 applied to P1-27, 25, 24, 22, 21, 20, 19, and 18. Each of these input lines that are at logic 1, represent a DCU address that receives a data word located in a specified register of the accessible memory data bank. At the beginning of the CCCS input/output cycle, a RESET logic 0 is received at P1-4, causing J-K flip-flops A8 and A7 to set. This action causes the input at pins 1, 14, and 15 of one-of-ten decoder A14 to be all logic 1. Because pins 2 and 8 of A14 are strapped to ground and outputs 6 and 7 are not used, the eight remaining outputs are controlled by the Q outputs of flip-flops A8B, A7A, and A7B. As the combination of 1's and 0's at pins 1, 14, and 15 of A14 vary, a logic 0 is applied to one of the outputs of decoder A14 and the remaining 7 outputs are at logic 1. The following listing indicates the inputs required at A14 to produce logic 0 at each of the eight outputs.

INPUT PINS			LOGIC 0
15	14	1	OUTPUT PIN
1	1	1	5
0	1	1	4
1	0	1	3
0	0	1	9
1	1	0	10
0	1	0	11
1	0	0	12
0	0	0	13

4-120. Decoder A14 outputs the logic 0 in the sequence shown in the above listing. Gates A13 and A19 invert these outputs and apply them to gates A23 and A18 for comparison with the EA1 through EA8 inputs. The ARC (address select clock) applied to P1-9 allows decoder A14 to sample the EA inputs by clocking J-K flip-flops A7 and A8. Each time a clock pulse is applied to pin 5 of A7B, the Q outputs of the counter applied to A14 also change and permit another EA to be sampled. When the decoder encounters an EA that is a logic 1, the ARC is inhibited and the $\bar{Q}$ outputs of A8B, A7A, and A7B are applied to pins 3, 4, and 5 of 8-input multiplexer A6. At the same time the CRA and CRB from accessible memory card A7A6 are applied to pins 1 and 2 of A6 through P1-10 and P1-11. The S1 and S2 at P1-5 and P1-3 originate on hardwire memory card and are determined by the program instruction. These bits are applied to pins 6 and 7 of 8-input multiplexer A6. The eighth input to A6 is the parity bit applied to P1-2 from processor timing card A7A4. These eight bits make up the 5-bit address group, the 2-bit subaddress group, and the parity bit illustrated in figure 4-3.

4-121. The seven address bits and the parity bit are read out serially at pin 15 of multiplexer A6 in response to inputs at pins 10, 11, 12, and 13 of A6. These inputs are derived from the CCCS timing counter composed of dual J-K flip-flops A2, A3, and A4. This counter establishes the time base for the CCCS bus control and monitor words. Timing for the 4-bit sync interval of carrier off, the dialogic bit, the 7-bit address field, and the 24-bit data field (figure 4-3) is provided by this CCCS timing counter. Before the eight bits of data in multiplexer A6 can be read out, the following conditions must be met.

a. Clock from the CCCS timing counter must be applied to pins 11, 12, and 13 of A6.

b. A logic 0 enable from A2A8 must be applied to pin 10 of A6.

c. A28B must be enabled by a logic 1 (dialogic bit) from A28C and the logic 0 output of A28A that is inverted by A12C.

d. A1C and A12C must be enabled by a logic 1 from pin 12 of input/output sequencer flip-flop A15A.

4-122. When the above conditions are met, the eight bits in multiplexer A6 are applied to the control data line at P1-26. As the eighth bit is read out of the multiplexer, the CCCS timing counter applies logic 0 to pins 1, 2, and 3 of A28A. The resulting logic 1 output causes the following:

a. Gate A12C is enabled.

b. Multiplexer A6 is inhibited by the logic 1 at pin 10 causing pin A6-15 to change to logic 0 and enable A28B.

c. The DBOT (data bank output retimed) at P1-36 is gated through A12C and A28B as bits 9 through 31 of the CCCS control word (figure 4-3).

4-123. After the CCCS bus control word leaves pin P1-26 of the CCCS timing card, the data is still at logic level and is routed to accessible memory card A7A6. The modulator section of this card modulates the data on a 4800-Hz sine-wave carrier and transmits on the CCCS control bus. The DCU addressed by the first five bits of the address field accepts the data, routes it to the DCFE's designated by the two subaddress bits that act upon the instructions contained in the 24-bit data field. After the DCU and DCFE's have acted upon the instructions, a response is generated by the DCU. This response is in the form of a CCCS bus monitor word (figure 4-3) and has the same address as the control word that caused the monitor response.

4-124. CCCS Receive Functions. The CCCS bus monitor words generated by the DCU's are received in the rom computer at accessible memory card A7A6 (figure 7-6). The data is demodulated to logic level and applied to the monitor data input at P1-32 of the CCCS timing card. The CCCS clock and the monitor gate inputs at P1-31 and P1-29 are also received from the demodulator section of accessible memory card A7A6. These inputs clock the 32-bit monitor word (figure 4-3) received from the DCU through a series of gates and flip-flops that make up the CCCS bus fault detector circuit. Each time a control word is transmitted on the CCCS bus, the fault detector circuit performs an automatic analysis routine to check for the presence of a monitor response on the CCCS monitor bus, compares the address of the monitor word received with the DCU address sent in the control word, checks for parity error, and checks for a power interrupt indication. If a no response or parity error occurs while the monitor word is sampled by the fault detector circuits, fault detector counter A27A/A27B causes the control word to be retransmitted and the DCU monitor word is again checked for the data link faults. This process is repeated three times and if the faults continue to appear, the detected fault data contained in dual J-K flip-flops A34 and A36 is clocked out of the FI line at P1-14 and is stored in the data bank fault register (register 16) on accessible memory card A7A6. The FIC is turned on and off by input/output sequencer flip-flops A15A/A15B. This clock output is used to clock the fault data into the data bank fault register.

4-125. Multiple Addressed Instructions. When an instruction word from hardwire memory contains more than one DCU address, the EA inputs to CCCS timing card A7A3 contain more than one logic 1. In these instances, the control word is transmitted to the first address encountered when decoder A14 is clocked by the ARC at P1-9. After the control word is transmitted to the first DCU address, the monitor word from the DCU is stored in a data bank register, and any detected

data link fault information is stored in the fault register; the CCCS timing counter enables decoder A14. When enabled, A14 selects the next address enable, inserts new address information in multiplexer A6, and transmits the 24-bit data field input from P1-36 to the second DCU address. The monitor response from the second DCU is processed in the same manner as that described for the first monitor word in paragraph 4-123. This process is repeated until each of the addresses enabled have been transmitted and each of the monitor responses stored. Then during the first bit of the next control word (the dialogic bit) RCT (return control transfer) at P1-6 goes to logic 0 and reinitiates the timing generated by the processor timing card. The processor timing circuits set SDT at P1-12 to logic 0, thereby causing the CCCS timing card to generate idle words.

4-126. PROCESSOR CARD CIRCUITS. Processor card A7A4 provides the basic timing for the internal operations of the rom computer. The following description is keyed to figure 7-10, a detailed logic diagram of the processor card circuits.

4-127. Timing Generator. Transistor Q2 and associated components functions as a 1-MHz oscillator and is the basic source of all internal timing signals used in the computer functions but is independent of the input/output timing. The output of the oscillator is applied through pulse shaper/delay AND gate A11 to a frequency divider network. This network consists of dual J-K flip-flops A12, A17, and A24. The flip-flops divide the 1-MHz input and produce three basic timing outputs. The $\overline{CLL}$ applied to pin P1-18 is a 256-kHz symmetrical square wave illustrated in figure 4-2. The Ø1 and Ø3 outputs at P1-33 and P1-19 present a one-of-four duty cycle time signal. The Ø1 has one part high and three parts low and the Ø3 signal has one part low and three parts high.

4-128. Other major timing signals used in the operation of the rom computer are the $\overline{WT1}$, $\overline{WT2}$, $\overline{WT4}$, $\overline{WT8}$, and $\overline{WT16}$ outputs applied to P1-26, 25, 27, 28, and 29. A $\overline{WT1}$ signal is 1 bit long and the $\overline{WT2}$, $\overline{WT4}$, $\overline{WT8}$, and $\overline{WT16}$ signals are 2, 4, 8, and 16 bits long respectively. These signals are derived from hexadecimal counters A13 and A18. Timing signals are clocked out of these counters by the clock signal from pin 9 of flip-flop A12B when gate A16A is enabled. In addition to the $\overline{WT1}$ through $\overline{WT16}$ outputs, pins 12 and 13 of counter A18 provide timing outputs as clock is applied to pin 2 of the counter. As the counter is clocked 0-0, 0-1, 1-0, and 1-1 combinations are applied to pins 12 and 13. The 0-0 at pins 12 and 13 of counter A18 define the instruction read frame. During this interval, clock signals are applied to the instruction storage registers on instruction decode card A7A5 and permit a new instruction to be read from hardwire memory card A7A2.

a. A 0-0 output also provides a logic 0 at pin 14 of A9D. This logic 0 is used to set flip-flops A2, A25A, and A25B on processor timing card A7A4 and is applied to P1-4 when it is extended to hardwire memory card A7A2, CCCS timing card A7A3, and instruction decode card A7A5 to perform various reset functions. In addition, the logic 0 is inverted by A8E that enables A10B and permits the INC (instruction storage clock) to be applied to P1-15. This clock signal is 32 bits long as illustrated in the waveform chart of figure 7-10.

b. At the next count, counter A18 has a 0-1 output at pins 12 and 13. This output defines the process time frame. During the short interval while pins 12 and 13 have the 0-1 output, the instruction that was read in the previous frame is executed by the computer. The 0-1 output places a logic 0 at pin 11 of A9C. The logic 0 is then applied to P1-5 as IDRT and is extended to accessible memory card A7A6 where it determines the process time interval. In addition, the IDRT signal enables the DBC applied to P1-17, and is gated with the OUTS signal at P1-24, the WT2, and the WT4 clock signals to provide one of the IAC clock enables. When the IDRT is gated with the EMB at P1-16, the accumulator clock is enabled during the process frame.

c. The next output of counter A18 is 1-0. This output defines the branch load frame if the BNZ + CNZ+COZ (conditional branch test signal) at P1-10 and the 0P0 at P1-30 is at logic 1 during any sample interval in the process frame. Otherwise the 1-0 output defines the increment load frame that is a 9-bit interval used to set up timing for the next instruction from memory. During this interval, a logic 0 is available at pin 8 of A19C that is inverted by A19D. The resulting logic 1 enables A15C, A20A, A15A, A5A, and A4B. With these gates enabled, the availability of BNZ+CNZ+COZ, OUTS, RCT, BPZ, and/or LCD inputs at P1-10, 24, 6, 21, and 13 determine whether outputs are applied to IAC CLOCK load

pulse at P1-31, ARC at P1-9, ACC (accumulator clock) at P1-20, or IAC CLOCK at P1-32.

d. The fourth output from pins 12 and 13 of counter A18 is 1-1. This output appears only when a branch load frame was previously initiated. The 1-1 output then becomes the increment load frame. During this interval, the new branch address that was loaded in the accumulator during the branch load frame is loaded into the instruction address counter. The 1-1 output also provides a logic 0 at pin 5 of A19B that is inverted by A19A. The resulting logic 1 enables A13D and permits an IAC LOAD PULSE (instruction address counter load pulse) to be applied to P1-39. A20B is also enabled and gates clock to pins 1 and 7 of flip-flop A21, causing the $\overline{Q}$ output at pin 12 to set counters A13 and A18.

4-129. As shown in figure 7-10, additional timing signals are derived from combinations of $\overline{WT1}$ through $\overline{WT16}$ outputs of hexadecimal counters A13 and A18. An example of such combinations is the EEL applied to pin P1-22. This signal is derived from a $\overline{WT8}$ and a $\overline{WT16}$ applied to NAND gate A10C. The output signal consists of 8 bits low and 24 bits high, the low representing the time interval of the 7 address bits and parity bit and the high representing the time interval of the 24-bit data field.

4-130. Data Bank Output Retiming Circuit. The DBO applied to P1-23 of the processor card is received from accessible memory card A7A6. Before this data is processed to the CCCS bus as control data, it is retimed to the 4800-Hz frequency of the CCCS processor clock signal. This signal is received from CCCS timing card A7A3 at P1-7. The signal is a 4800-Hz square wave that clocks the DBO out of retiming flip-flop A1 and applies the DBOT to pin P1-36. The DBOT is then extended to CCCS timing card A7A3 (figure 7-9) where the serial data is combined with the 7-bit address field and the parity bit to form the 32-bit CCCS bus control word. The parity bit is derived from flip-flop A25B on the processor timing card. Each bit of the DBO received at P1-23 is sampled by flip-flop A25B. If there is an even number of logic 1 in the DBO 24-bit data field, the parity output at P1-2 is logic 0 and if there is an uneven number of logic 1 in the data field, a logic 1 is applied to P1-2.

4-131. Power Interrupt Circuit. The power interrupt circuit consists of transistors Q1, Q3, and Q4 along with associated components. There are two conditions that activate the power interrupt circuit; an interruption of the +5-volt dc power or a logic 0 applied to the FINS input at P1-11. When the +5-volt dc power is interrupted, a logic 0 is applied to the base of transistor Q3 activating the power interrupt driver circuit. As Q3 starts to conduct, C3 charges and, during this interval, a logic 0 is applied to pin 12 of A26D and to pin 10 of A26C. The time duration of the logic 0 is sufficient to apply a logic 0 at pin 11 of A27C that is extended to P1-8 and hardwire memory card A7A2 where it is used to reset the instruction address counter to 0.

4-132. The FINS input at P1-11 originates at the read verifier circuit of hardwire memory card A7A2. Instruction words from memory are read out twice and compared. When the two readings compare, a logic 1 is received at P1-11 and the power interrupt output at P1-8 is at logic 1 because pin 11 of A27C is also at logic 1. When the instruction words do not compare, a logic 0 is applied to the FINS input. This condition applies a logic 1 to the base of Q1, resulting in a logic 0 at pin 12 of A26D and pin 10 of A26C. The output of A27C is also at logic 0, causing a power interrupt signal to reset the instruction address counter.

4-133. TRANSMIT AND RECEIVE CONTROL HEAD POWER SUPPLY CIRCUITS.

4-134. Dc low voltage required to operate the transmit and receive control heads is obtained from power supplies A7A10PS1 and A8A5PS1 on the control head rear panels (figure 4-1). These power supplies are identical but operate independently. Primary power is applied to the power supplies through the audio control unit. The power supplies convert 120 volts ac, ±10%, 47- to 420-Hz to the dc voltages shown in table 4-11. The power supply provides these voltages when loaded from 30% to 100% full load.

Table 4-11. Transmit and Receive Control Head Power Supply Outputs

NOMINAL VOLTAGE AND CURRENT	NOMINAL OPERATING VOLTAGE RANGE	ABSOLUTE MAXIMUM
+5 Vdc @ 3 A	4.75 to 5.25 V	+6.5 V
+12 Vdc @ 150 mA	11 to 13 V	+15.6 V
-25 Vdc @ 200 mA	-24 to -27 V	-28.0 V
+4.3 Vdc @ 1.5 A	3.8 to 4.7 V	+6.0 V

4-135. Control circuits in the power supply regulate the output voltages to within the specified operating ranges with ac input variations from 108 to 132 volts ac. Overload and overvoltage protection is also provided. Referring to the schematic diagram shown in figure 7-11, the 120-volt ac input is rectified by full-wave bridge rectifiers CR1 through CR4 and filtered by the capacitive-input filter section of C1 through C4, L1, and C24. Approximately 150 volts dc is developed across C24. This high-level dc voltage is converted to the four lower output supply voltages by the switching stage of Q1 and Q2 and the independent rectifier and filter circuits connected to the secondary windings of T1. The secondary winding of T1 at terminals 7, 8, and 9, and bridge rectifiers CR17 through CR20 provide supply voltages, proportional to the output supply voltages, to the voltage, overload, and overvoltage control stages. The voltage control stage consists of linear differential amplifier Q9 and Q10, zener diode CR21, and associated circuit components. The overload control stage consists of Q6, Q7, and Q8. Normally Q7 and Q8 are off and diode connected transistor Q6 provides temperature stabilization for the stage. Nonlinear (on/off) differential amplifier Q4 and Q5, and zener diode CR22 form the overvoltage control stage.

4-136. In this stage, Q4 is normally on while Q5 is off. The voltage and overload control stages vary the forward bias of the bias control stage of Q11. Transistor Q11, in turn, varies the forward bias of Q1 and Q2 by varying the drive current through the feedback winding of T1 (4, 5, and 6), emitter base junction of Q11, R25, and R24 to the positive side of C24. Thus biased, current begins to flow through Q1 and Q2. Because no two transistors are electrically identical, one transistor conducts more than the other. This difference current, or starting current, causes a small voltage to be induced in the feedback winding connected to the bases of Q1 and Q2. The polarity is such that the more conducting transistor conducts even more heavily (positive feedback). This process continues until approximately 112 volts is developed across the primary winding of T1 associated with the conducting transistor. The primary voltage of T1 is limited at this value by the negative feedback action of the voltage control stage, which varies the bias of Q11 and in turn Q1 and Q2. The combination of the negative feedback from the voltage control stage and the positive feedback from the feedback winding of T1 results in a linear increase in the conducting transistor collector current. The primary current of T1, therefore, is changing at a constant rate, thus keeping a constant 112 volts across the primary winding during this interval. Primary current and the resultant core flux of T1 continues to increase at a constant rate until core saturation is reached. Because there is no further flux buildup at core saturation as the primary current continues to increase, the induced secondary voltages drop to zero. This action removes the positive feedback voltage, and the conducting transistor collector current decreases, causing an induced voltage of opposite polarity. The process then reverses so that the previously nonconducting transistor starts to conduct and the previously conducting transistor becomes cut off. Transistors Q1 and Q2 are not operated at saturation so that 112 volts is developed across each alternate primary winding of transformer T1 regardless of ac input variations

from 108 to 132 volts ac. The result is a regulated square wave of 224 volts peak-to-peak across the windings of T1. In turn, regulated stepped-down voltages are induced into the secondary windings of T1, and are rectified and filtered to provide the output supply voltages. The output voltage level is determined by the adjustment of output adjustment potentiometer R20.

4-137. Overload protection with automatic recovery is provided by the overload stage if the full-rated input power of approximately 50 watts is exceeded by 25 percent. This includes protection against continuous short circuits. In the event of overloads in excess of 125 percent of the rated input power, the output voltages approach zero. Assuming such an overload exists, the current through current sensing resistor R2 develops sufficient voltage across R2 to cause Q7 and in turn Q8 to conduct. When Q8 conducts, forward bias decreases for Q11 and in turn Q1 and Q2, causing the output voltages to approach zero. A bendback relationship exists when the overload stage is controlling the current through Q1 and Q2 in that the current through R2 is reduced (bentback) to less than half of its original full-rated dc input current value. The power supply input power is also reduced to less than half of the full-rated power value under overload conditions. With the reduced T1 secondary voltages, the reduced voltage across R2 is still sufficient to keep Q7 conducting, and the power supply remains in this condition until the load returns to normal. When the load returns to normal, less voltage is developed across R2, causing Q7 and Q8 to cut off. With Q8 cutoff, the bias of Q1 and Q2 is then determined by the voltage control stage, which causes the normal output supply voltages to be restored.

4-138. Output overvoltage protection is provided by the overvoltage control stage. If the output voltages exceed the maximum limits listed in table 4-11 due to excessively high ac input voltage or failure of the voltage control stage, transistor Q5 conducts and fires scr Q3. With Q3 conducting, the high-level dc voltage across C24 is short circuited (crowbared), which blows the fuse in the ac line to the power supply. The point at which Q5 conducts is determined by the adjustment of the overvoltage adjustment potentiometer R10.

4-139. AUDIO CONTROL UNIT CIRCUITS. The audio control unit, shown as a separate section of the radio control group in figure 4-1, provides the electrical and physical interface for the transmit and receive control heads. In addition, the unit contains the circuits required to operate the radio equipment after it has been turned on and set up by the two control heads. The following circuit descriptions are keyed to the schematic diagrams of the audio control unit shown in figure 7-12.

4-140. POWER CIRCUITS. Connector J2, on the rear of the audio control unit, provides the input for the 120-volt ac power that operates all the circuits of the radio control group. Filters FL1 and FL2 are installed in the ac lines between connector J2 and terminal board TB1 to reduce electromagnetic interference in the control group circuits. Circuit breaker CB1 is a single-pole breaker that serves as a front panel ON/OFF switch and overload protection. Terminal board TB1 is a distribution point for the ac voltage. One branch of the 120-volt ac power is applied to power supply PS1. This power supply is a sealed unit that provides 24 volts dc to operate amplifiers A2, A3, A4, A5, and A6. A second branch of the 120-volt ac power is routed through DIM resistor R42 that varies the voltage applied to the edge-lighting panels of the audio control unit and the transmit and receive control heads. Figure 7-12 shows how the dimmed 120 volts ac is applied directly to the edge-lighting panel on the audio control unit and through connectors P3 and P4 to the transmit and receive control heads. The primary 120-volt ac line is also extended to the control heads through connectors P3 and P4 and to fan B1. The blackout strap between pins F and G of connectors P3 and P4 are provided in lieu of an external switch to control the on/off operation of the edgelighting circuits.

4-141. AUDIO CIRCUITS. Four transmit channels, four receive channels, a monitor bus, and an order-wire circuit are controlled and operated from the audio control unit. Switches S2 through S5 select the channels to be operated or monitored, and switch S6 controls operation of the order wire. Amplification for the transmit audio lines is provided by microphone amplifier A4, agc amplifier A3, and line amplifier A2. Received audio is amplified by line amplifier A5 when switch S7 is in the HDST position. If speaker LS1 is used to receive, the audio switch S7 is set to SPKR selecting line amplifier A2 and speaker amplifier A6 to provide the audio amplification. The fixed resistors, used in the impedance networks of the audio circuits, are on circuit card A1. This circuit card is a plug-in type that contains only the resistors

and interconnections shown in figure 7-12. Variable resistor R41 is a front panel VOL control that adjusts the volume of the audio received at speaker LS1 or an external headset.

4-142. TRANSMIT AND RECEIVE CONTROL HEAD INTERFACE CIRCUITS. Refer to figure 7-12. Connectors P1 and P2 are on pendant cables that provide the signal interface with the transmit and receive control heads. Strapping between these two internal connectors complete circuits of the logic level bus between the two control head front panels and the rom computer. Connector P1 also connects the CCCS bus to connector J1 on the rear of the audio control unit. These internal connectors are routed through filters FL3, FL4, and FL5 and carry the data transmitted by the rom computer or received from the DCU's of the radio equipment. Other interface functions at connectors P1 and P2 are described briefly below and are illustrated in figure 7-12 and the other illustrations specified.

a. The key strap between pins P1-22 and P1-26 provides continuity between the KEY-OFF-VOX/PTT switch on the front panel of the transmit control head (figure 7-1) and the key input at pin P1-12 of the matrix card (figure 7-3). This circuit is a transmit function only and enables or disables the CCCS transmitter key circuit by applying or removing ground (logic 0) at P1-12 of the matrix card.

b. The lamp test straps between pins 42 and 44 of P1 and P2 provide continuity between the lamp test 1 and lamp test 2 lines at P1-52 and P1-54 of the logic level slave card (figure 7-5). This continuity permits ground (logic 0) to be applied to all the lamp driver circuits simultaneously when the LAMP TEST switch on the respective control head is pressed.

c. The radio group 2 strap between pins 43 and 48 of audio control unit P1 and P2 provide a continuous ground (logic 0) at pin P1-64 of the logic level slave card. This logic 0 is required to operate the one-of-sixteen decoder circuit shown in figure 7-5 and described in paragraph 4-88.

d. The receiver through coupler strap between pins 25 and 39 of audio control unit connector P1 provides a constant ground (logic 0) at P1-7 of the matrix card (figure 7-3). This logic 0 keeps bit 8 of transmit logic level monitor word 2 (table 4-2) at logic 0, causing the antenna coupler to be bypassed in receive operation.

e. Simplex entry at audio control unit connector P1 is the computer entry for simplex and duplex operation. SIMPLEX/DUPLEX switch S1 applies or removes ground (logic 0) to P1-24 and this signal is extended to P1-D of the matrix card (figure 7-3). Therefore, switch S1 controls the condition of bit 3 in transmit logic level monitor word 2 (table 4-2) that selects either simplex or duplex operation.

f. VOX entry at audio control unit connector P1-23 is a computer entry for VOX or cw/ptt keying. VOX-CW/PTT switch S8 applies or removes ground (logic 0) to P1-23 and this signal is extended to P1-3 of the matrix card (figure 7-3). Therefore, switch S8 controls the condition of bit 2 in transmit logic level monitor word 2 (table 4-2) that selects VOX keying by the radio equipment or enables the cw and ptt lines. This switch also opens the ptt keyline when the VOX mode of operation is selected.

g. Keying interlock circuits between the front panel switches and circuits on the audio control unit are completed through pins 28, 29, 30, 31, 32, and 33 of audio control unit connector P1. Because connector P1 mates with connector J1 of the audio control unit, reference to figures 7-12 and 7-1 explains the relationship of the transmit control head front panel switches with switch S8 and jacks J3 and J4 of the audio control unit. Refer to paragraphs 4-50 and 4-53 for more information on the interlock circuits.

4-143. RADIO CONTROL GROUP INTERFACE CIRCUITS. All the circuits of the radio control group except the primary power are interfaced with the radio equipment and/or unique system equipment through connector J1 on the rear of the audio control unit. Figure 7-12 shows the exact connections of these inputs and outputs. Primary communications between the rom computer and the radio equipment DCU's is via the CCCS bus. This bus includes six shielded pairs for the carrier (clock) bus at pins J1-y and J1-AA, the control bus at pins J1-CC and J1-DD, and the monitor bus at pins J1-FF and J1-GG. The ptt keyline at pins J1-x and J1-y is external to the CCCS bus and provides a means for keying the radio transmitter in addition to the key capabilities of the CCCS bus.

4-144. The four independent-sideband channels account for eight additional wire pairs. Four receive lines are inputs of connector J1 at pins U, V, W, X, Y, Z, a, and b. These inputs are

routed through impedance networks before they are applied to switches S2 through S5. The monitor bus at pins H and J of connector J1 are also routed through switches S2 through S5 and permit the operator to monitor the input from speaker LS1 or an external headset. The four transmit sideband channel outputs at K-L, M-N, P-R, and S-T of connector J1 permit voice transmissions from jack J3 of the audio control unit. The CW KEY jack J4 provides an input to the ptt keyline to key the oscillator and exciter when cw operation is selected. An order-wire transmit and receive wire pair is interfaced at pins F and G of connector J1. ORDER WIRE switch S6 is a momentary switch that must be held in the TALK position for transmission on the order wire. When released, the switch returns to OFF, but must be manually placed to LISTEN (a locking position) to monitor order-wire communications.

4-145. Six wire pairs terminated at connector J1 of the audio control unit are shown as test points in figure 7-12. These test points connectors are brought out to the interface connector to facilitate extention to jackfields or other suitable means of system application or testing. The test points permit measurement of input and output levels for the amplifiers of the audio control unit. Although the amplifiers are sealed units, each amplifier is equipped with a GAIN adjust, and holes in the audio control unit chassis permit access for level adjustments when required. However, the gain of the amplifiers are preset at the factory and normally should not require adjustment during field operations. Power supply PS1 is also a sealed unit that cannot be repaired. Like the amplifiers, the power supply is also equipped with an output adjustment but normally will not require adjustment in the field.

SECTION III

FUNCTIONAL OPERATION OF MECHANICAL ASSEMBLIES

NOT APPLICABLE

CHAPTER 5

MAINTENANCE

5-1. INTRODUCTION. Control-Monitor Group OK-145/TSC-60(V) (radio control group) is designed primarily for operation in communication centrals of the AN/TSC-60(V) series. Within the maintenance concept established for the AN/TSC-60(V) series, maintenance testing is accomplished using the related communication central as a test-bed to fault-isolate to a slice (module) or, in some cases, to a card. Maintenance information for the radio control group is contained in the following manuals.

T.O. 31S1-2TSC60-2 - Technical Manual, Service, Communication Central AN/TSC-60(V)1

T.O. 31S1-2TSC60-12 - Technical Manual, Service, Communication Centrals AN/TSC-60(V)2 and AN/TSC-60(V)3.

CHAPTER 6

ILLUSTRATED PARTS BREAKDOWN

SECTION I

INTRODUCTION

6-1. GENERAL.

6-2. This Illustrated Parts Breakdown (IPB) lists, illustrates, and describes assemblies, subassemblies, and detail parts for equipment manufactured by Collins Radio Company. (See figure 6-1.)

6-3. The IPB provides information for requisitioning, stocking, issuing, and identifying parts, and illustrates assembly and disassembly relationship.

6-4. This IPB is to be used in conjunction with the following publications:

Illustrated Parts Breakdown
Communication Central AN/TSC-60(V)1
T.O. 31S1-2TSC60-4

Illustrated Parts Breakdown
Communication Centrals AN/TSC-60(V)2 and AN/TSC-60(V)3
T.O. 31S1-2TSC60-14

6-5. CONTENT.

6-6. The IPB is divided into four sections: Introduction, Group Assembly Parts List, Numerical Index, and Reference Designation Index.

6-7. The Collins Radio Company part numbering system is composed of a 3-digit family number, a 4-digit serial number, and a 3-digit dash number.

6-8. Terms and abbreviations used in the preparation of the IPB are defined as follows:

a. NHA: The NHA notation following the description of a part means the next higher assembly of that part.

b. SEE FIG: The SEE FIG. notation following the description indicates that the item and its component parts are shown in detail in the figure indicated.

c. CI (configuration identifier) is recorded on each chassis and/or replaceable assembly. CI is designated by a 5-digit number consisting of:

FISCAL YEAR	WEEK	DAY
71	40	7

CI effectivity (EFF) is recorded by a notation in the description:

/EFF TO CI_____/indicates part is used in chassis/assembly prior to given CI.

/EFF CI_____ TO CI_____/indicates usage beginning with first CI and continuing to but not including second CI.

/EFF WITH CI_____/indicates usage beginning with given CI and continuing to present production.

d. All other abbreviations used in this IPB are in accordance with MIL-STD-12C.

6-9. If repair parts are to be supplied in the form of a kit, the kit appears as the last entry in the applicable breakdown. Kits are not illustrated or broken down.

6-10. SOURCE AND REPAIR CODE.

6-11. Policies, general information, and procedures for changing source and maintenance coding are contained in T.O. 00-25-195. Generally, the source codes and maintenance repair level codes herein (see SOURCE CODE and REPAIR CODE columns) were assigned by Air Force Personnel when this equipment was purchased. Assignment of codes was influenced by maintenance policies of the Air Force base self-sufficiency program, predicted maintenance actions, base facilities and capabilities, and economic considerations. Definitions of these codes follow.

6-12. CODE P - PARTS UNDER INVENTORY STOCK CONTROL.

a. Code P applies to parts on which usage is anticipated or known. Code P parts can be requisitioned and installed by any maintenance level consistent with the Command's authorized scope of maintenance. Restricted service manufacture is considered practicable but only after an attempt has been made to procure from supply sources.

b. Code PD identifies parts that can be requisitioned and installed by Air Force activities authorized depot level maintenance only. Restricted service manufacture of PD coded parts is considered practicable but can be accomplished only after confirmation of nonavailability from supply sources.

c. Code P1 identifies parts that are very difficult or uneconomical to manufacture. Service manufacture is considered impracticable. Code P1 parts can be requisitioned and installed by any maintenance level.

d. Code P1D applies to items that are restricted to depot level requisition and/or replacement only.

e. Code P2 identifies insurance-type spare parts that can be installed by any Air Force activity consistent with the Command's authorized scope of maintenance. This code applies to parts that are basically structural and for which no usage is anticipated or known; require special tools, templates, and/or jigs; or are very difficult, impractical, or uneconomical to manufacture by an Air Force activity. These items are not subject to periodic replacement or wearout but may require infrequent replacement as a result of accident or other unexpected occurrences. Delayed procurement items, as defined in AFLCM 400-1, are included under this code.

f. Code P2D applies to insurance-type items issued and installed at depot level only. This code is applied to parts as described under Code P2 and to delayed procurement items referenced in AFLCM 400-1.

6-13. CODE M - PARTS NOT PROCURED.

a. Code M applies to parts that can be manufactured within the facilities of any activity. Procurement and stocking of these parts are not justified in view of the relatively low usage, or storage and installation factors. Needs are to be met by local manufacture as required.

b. Code M1 applies to parts that can be manufactured only by using the facilities of the depot (O and R) activity. Procurement and stocking of these parts are not justified in view of their relatively low usage and installation factors. The needs of all activities are to be met through salvage or by depot (O and R) level manufacture.

6-14. CODE A - ASSEMBLY NOT PROCURED.

a. Code A applies to assemblies made up of two or more units, one of which is purchased and carries an individual part number and description and which can be assembled by any maintenance level.

b. Code A1 applies to assemblies made up of two or more parts, each of which carries an individual part number and description and which may be assembled only by activities having depot (O and R) facilities.

6-15. CODE X - PARTS CONSIDERED IMPRACTICABLE FOR MANUFACTURE OR PROCUREMENT.

a. Code X applies to main structural members or similar parts that, if required, would suggest extensive equipment reconditioning. The need of a part(s) coded X should normally result in a recommendation to retire the article from service.

b. Code X1 applies to parts for which procurement of the next larger assembly is justified; for example, an integral part, such as welded segments, inseparable from its assembly; a part machined in a matched set; or a part of an assembly that, if required, would suggest extensive reconditioning of each assembly.

c. Code X1D identifies parts described under Code X1 but which are applicable to Air Force activities authorized depot level maintenance only.

d. Code X2 is applied to parts that are neither procured nor stocked. Activities requiring such parts shall attempt to obtain them from salvage; if not obtainable from salvage, such parts shall be requisitioned through normal supply channels with supporting justification.

e. Code X2D identifies parts described under Code X2 but which are applicable to Air Force activities authorized depot level maintenance only. Repeated requests for such parts shall justify a change to Code P1D or P2D, as applicable, if considered economical and feasible to procure and stock such parts.

6-16. CODE U - PARTS NOT PROCURED, MANUFACTURED, OR STOCKED. Code U applies to installation drawings, diagrams, instruction sheets, field service drawing numbers, and parts not otherwise of supply significance, including obsolete parts that cannot be procured or service manufactured.

6-17. CODE C - CURE-DATED COMPONENT KITS. Code C applies to cure-dated kits containing replacements for parts subject to deterioration because of aging or exposure to aromatic fuels, such as rubber gaskets, seals, packings, and O-rings. Kits coded C may include noncure-dated gaskets, packings, etc., necessary for reassembly after service change or bulletin compliance.

6-18. CODE D- MAJOR OVERHAUL KIT. Code D applies to overhaul kits that are available only to activities authorized to perform depot or major overhaul. These kits do not contain cure-dated parts.

6-19. CODE F - MINOR OR FIELD REPAIR KIT. Code F applies to kits that are available to maintenance activities authorized to perform minor or field repair, including overhaul activities in support of field activities.

6-20. CODE KC - COMPONENT OF C KIT. Code KC applies to items that are components of C kit; these items are also stocked separately in the appropriate class if followed by the letter P.

6-21. CODE KD - COMPONENT OF D KIT. Code KD applies to items that are components of D kit; these items are also stocked separately in the appropriate class if followed by the letter P.

6-22. CODE KF - COMPONENT OF F KIT. Code KF applies to items that are components of F kit; these items are also stocked separately in the appropriate class if followed by the letter P.

6-23. CODE KB - COMPONENT OF BOTH F KIT AND D KIT. Code KB applies to items that are components of both F kit and D kit; these items are also stocked separately in the appropriate class if followed by the letter P.

6-24. CODE S - NO REPAIR. Code S identifies items that are nonrepairable and have no reclamation value. When these items fail, they must be disposed of at user level as condemned material.

6-25. CODE B - NO REPAIR; RECONDITION; BASE DISPOSAL. Code B identifies assemblies or parts that must be reconditioned at user level by adjusting, cleaning, soldering broken connections, etc. If these items cannot be returned to serviceable condition by such means, they must be disposed of at user level as condemned material. No repair parts or tools are specially procured for maintenance of these items.

6-26. CODE F - FIELD LEVEL MAINTENANCE; BASE DISPOSAL. Code F identifies items that are repaired by the field level maintenance activities or contracted for repair at base level IAW T.O. 00-25-68. Normal servicing must be done by organizational level maintenance. Selected parts, tools, and technical order data are procured and provided to applicable level maintenance activities for repair of these items. No specialized repair activity (SRA) is established for these items. If they cannot be returned to serviceable condition by the field level maintenance activity with the parts and tools provided, they must be disposed of as condemned material. Hi-value and critical items, however, must be turned in to supply, and disposition instructions obtained from the applicable IM.

6-27. CODE D - LIMITED REPAIR; DEPOT OVERHAUL AND DISPOSAL. Code D identifies items on which a limited degree of repair can be accomplished by field level maintenance activities. SRA is established for overhaul of these items. A range of repair parts, tools, and technical order data consistent with the capability of repair are procured and provided to applicable field maintenance activities. Because of the design characteristics and complexity of repair, the degree of repair that is authorized on these items at field level maintenance is necessarily determined by the degree of technical skills required and the cost of special tools, special test equipment, spare parts, and the predicted frequency of failure generation. If these items cannot be returned to serviceable condition with authorized parts and tools, return them to supply for shipment to the designated SRA.

6-28. CODE DM - LIMITED FIELD REPAIR; MOBILE DEPOT OVERHAUL. Code DM identifies items to which all the conditions of Code D apply except that repair beyond field capability is done by the Mobile Depot Activity (MDA). If the MDA cannot repair these items, MDA determines whether these items should be condemned or sent to the SRA.

6-29. CODE L - DEPOT LEVEL MAINTENANCE ONLY. Code L identifies items that are repaired only by designated SRA. Repair parts and tools for repair are procured and provided only to these authorized activities. Required functional checkout and bench check equipment may be provided to applicable organizational and field level maintenance activities for accomplishing external adjustment or calibration and for verifying serviceability of these items. If they are found unserviceable, return them to supply for shipment to the SRA.

6-30. CODE LM - DEPOT LEVEL MAINTENANCE ONLY. Mobile Depot Activity Code LM identifies items to which all conditions of Code L apply except that repair is accomplished by MDA. If MDA cannot repair these items, MDA determines whether these items should be condemned or sent to the SRA.

6-31. LIST OF MANUFACTURERS.

6-32. This list does not include the prime contractors code (13499, Collins Radio Company, Cedar Rapids, Iowa), which does not appear in the Group Assembly Parts List. The codes reflected in this IPB, arranged numerically, are as follows:

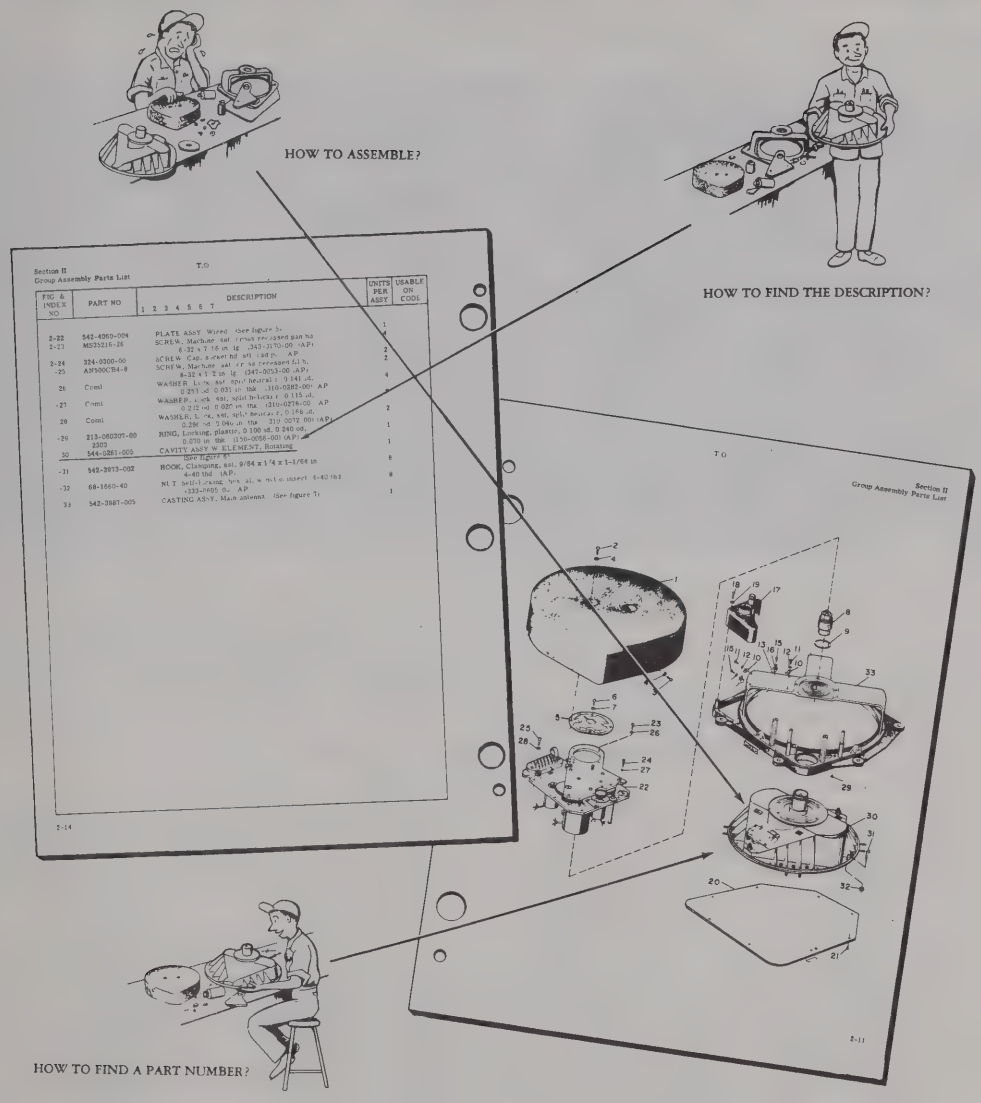
CODE	NAME AND ADDRESS
00779	Amp, Inc. PO Box 3608 Harrisburg, PA 17105
01121	Allen Bradley Co. 1201 S Second St. Milwaukee, WI 53204
01295	Texas Instruments, Inc. Components Group PO Box 5012 13500 N Central Exp. Dallas, TX 75222
01939	See 56289
02660	Bunkerramo Corp. Amphenol Connector Div. 2801 S 25th Ave. Broadview, IL 60153
04211	Coastal Dynamics Corp. 219 Rose Ave. Venice, CA 90291
06383	Panduit Corp. 17301 Ridgeland Tinley Park, IL 60477
06973	Angerman Heating, Inc. Denver, CO.
07125	See 80406
07263	Fairchild Camera and Instrument Co. Semiconductor Div. 464 Ellis St. Mountain View, CA 94040
07933	Raytheon Co. Semiconductor Div. Hq. 350 Ellis St. Mountain View, CA 94040
07886	National Radio, Inc. Commercial Products Div. 37 Washington St. Melrose, MA 02176
09922	Burndy Corp Richards Ave. Norwalk, CT 06852
12040	National Semiconductor Corp. Commerce Dr. PO Box 443 Danbury, CT 06810
13103	Thermalloy Co. 8717 Diplomacy Row Dallas, TX 75247
13606	See 56289
13850	Technipower, Inc. 18 Marshall St. South Norwalk, CT 06854

CODE	NAME AND ADDRESS
14936	General Instrument Corp. Semiconductor Products Group PO Box 600 600 W John St. Hicksville, NY 11802
16299	Corning Glass Works Electronic Components Div. 3900 Electronics Dr. Raleigh, NC 27604
16319	All States Nameplate Co., Inc. 228 Yorktown St. Dallas, TX 75208
16546	U.S. Capacitor Corp. 2151 N Lincoln Burbank, CA 91504
17117	Ideas, Inc. PO Box 2348 Santa Fe, NM 87501
17537	Lamps, Inc. 19220 S Normandie Ave. Torrance, CA 90502
24455	General Electric Co. Lamp Div. of Consumer Products Group Nela Park Cleveland, OH
27014	National Semi-Conductor Corp. 2950 San Ysidro Way Santa Clara, CA 95051
27074	United Electric Motor Co., Inc. 4354 Industrial Center San Antonio, TX 78217
44655	Ohmite Mfg. Co. 3601 W Howard St. Skokie, IL 60076
45722	Parker-Kalon Corp. Enten Rd. Clifton, NJ 07011
46384	Penn Engineering and Mfg. Corp. Old Easton Hwy. Doylestown, PA 18901
49956	Raytheon Co. 141 Springs St. Lexington, MA 02173
56289	Sprague Electric Co. North Adams, MA 01247
61957	USM Corp. 140 Federal St. Boston, MA 02107
64294	Webster Electric Co., Inc. 1900 Clark St. Racine, WI 53403
70318	Allmetal Screw Products Co., Inc. 821 Stewart Ave. Garden City, NY 11530
70674	ADC Products Div. of Magnetic Controls Co. 4900 West 78th St. Minneapolis, MN 55435
71785	Cinch Mfg. Co. and Howard B. Jones Div. 1026 S Homan Ave. Chicago, IL 60624
72606	Gasket Mfg. Co. 319 W 17th St. Los Angeles, CA 90015
72619	Dialight Corp. 60 Stewart Ave. Brooklyn, NY 11237
72765	Drake Mfg. Co. 4626 N Olcott Ave. Harwood Heights, IL 60656
72794	Dzus Fastener Co., Inc. 425 Union Blvd. West Islip, NY 11795
72962	Elastic Stop Nut Div. of Amerace Esna Corp. 2330 Vauxhall Rd. Union, NJ 07083
74199	Quam Nichols Co. 218 E Marquette Rd. Chicago, IL 60637

CODE	NAME AND ADDRESS
74921	The Iten Fibre Co. 4001 Benefit Ave. PO Box 9 Ashtabula, OH 44004
77250	Pheoll Manufacturing Co. Div. of Allied Products Corp. 5700 W Roosevelt Rd. Chicago, IL 60650
77820	Bendix Corp. The Electrical Components Div. Sherman Ave. Sidney, NY 13838
78189	Illinois Tool Works, Inc. Shakeproof Div. St. Charles Rd. Elgin, IL 60126
79607	Wilkes Barre Carriage Co., Inc. New York, NY
79807	Wrought Washer Mfg. Co. 2100 S Bay St. Milwaukee, WI 53207
81541	Airpax Electronics, Inc. Woods Rd. Cambridge, MD 21613
81640	Controls Co. of America Control Switch Div. 1420 Delmar Dr. Folcroft, PA 19032
82877	Rotron, Inc. 7-9 Hasbrouck Lane Woodstock, NY 12498
83003	Varo, Inc. 800 W Garland Ave. Garland, TX 75040
83014	Hartwell Corp. 9035 Venice Blvd. Los Angeles, CA 90034
83324	Rosan, Inc. 2901 W Coast Hwy Newport Beach, CA 92633
86928	Seastrom Mfg. Co., Inc. 701 Sonora Ave. Glendale, CA 91201
91637	Dale Electronics, Inc. PO Box 609 Columbus, NB 68601
93332	Sylvania Electric Products, Inc. Semiconductor Products Div. 100 Sylvan Rd. Woburn, MA 01801
96733	San Fernando Electric Mfg. Co. 1501 First St. San Fernando, CA 91341
97564	Clarependar, Inc. PO Box 785 Post Falls, ID 83854
98291	Sealectro Corp. 225 Hoyt Mamaroneck, NY 10544
99378	Atlee Corp. Lowell Ave. Winchester, MA 01890

HOW TO USE THIS ILLUSTRATED PARTS BREAKDOWN

SHEET 1 OF 2



HOW TO FIND THE PART NUMBER IF THE SECTION OR SYSTEM OF THE EQUIPMENT IN WHICH THE PART IS USED IS KNOWN:

(1) Turn to the Table of Contents and find the page number for the major assembly or system in which the part is used.

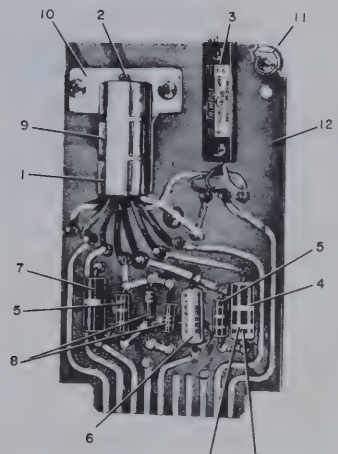
(2) Turn to the page determined in step (1).

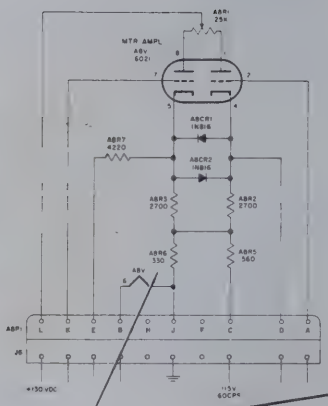
(3) Locate the part and its index number on the illustration.

(4) Find the index number on the Group Assembly Parts List page to determine complete description.

HOW TO USE THIS ILLUSTRATED PARTS BREAKDOWN

SHEET 2 OF 2





Section III
Numerical Index

T.O.

PART NUMBER	FIGURE & INDEX NUMBER	QTY PER ART	SOURCE CODE
RC32GF223K	24-92	1	
RC32GF271K	37-9[illegible]	1	
RC32GF272K	71-31	1	
RC32GF331K	23-4	1	
RC32GF333K	24-106	1	
RC32GF392K	71-32	1	
RC32GF393K	24-109	1	
RC32GF471K	66-72	1	
RC32GF473K	24-10	1	
RC32GF561K	23-	1	
RC32GF562K	70-7	1	
RC32GF682K	24-1	1	
RC32GF822K	24-		
RC42GF100K	83-		
RC42GF101K	59-10		
RC42GF103K	92-		
RC42GF104K	75-32		
	76-32		
	84-101		
	93-47		
	45-10		
RC42GF123K	46-10		

Section IV
Reference Designation Index

T.O.

REFERENCE DESIGNATION	FIGURE & INDEX NO.	PART NUMBER
A7T1	22-28	
A7T2	22-27	X-065
A8CR1	23-8	X-077
A8CR2	23-8	1N816
A8P1	23-12	1N816
A8R1	23-3	546-7884-004
A8R2	23-5	224L-1-203
A8R3	23-5	RC20GF272K
A8R5	23-7	RC20GF272K
A8R6	23-4	RC32GF561K
A8R7	23-6	RC32GF331K
A8V1	23-2	RN65B4221F
CR1	24-111	6021
CR2	24-111	JAN-1N251
CR3	24-111	JAN-1N251
CR4	24-111	JAN-1N251
CR5	24-111	JAN-1N251
CR6	24-111	JAN-1N251
CR7	24-111	JAN-1N251
C10	24-110	1N198

REFERENCE DESIGNATION	F I
3A3R10	
3A3R11	
3A3R13	
3A3R14	
3A3R15	
3A3R16	2
3A3R17	2
3A3R18	2
3A3R19	2
3A3R2	24
3A3R20	24
3A3R21	24
3A3R22	22
3A3R23	25
3A3R28	22
3A3R29	25
3A3R29	24

HOW TO FIND THE ILLUSTRATION FOR A PART IF THE PART NUMBER IS KNOWN:

(5) Refer to section III, the Numerical Index, and find the part number.

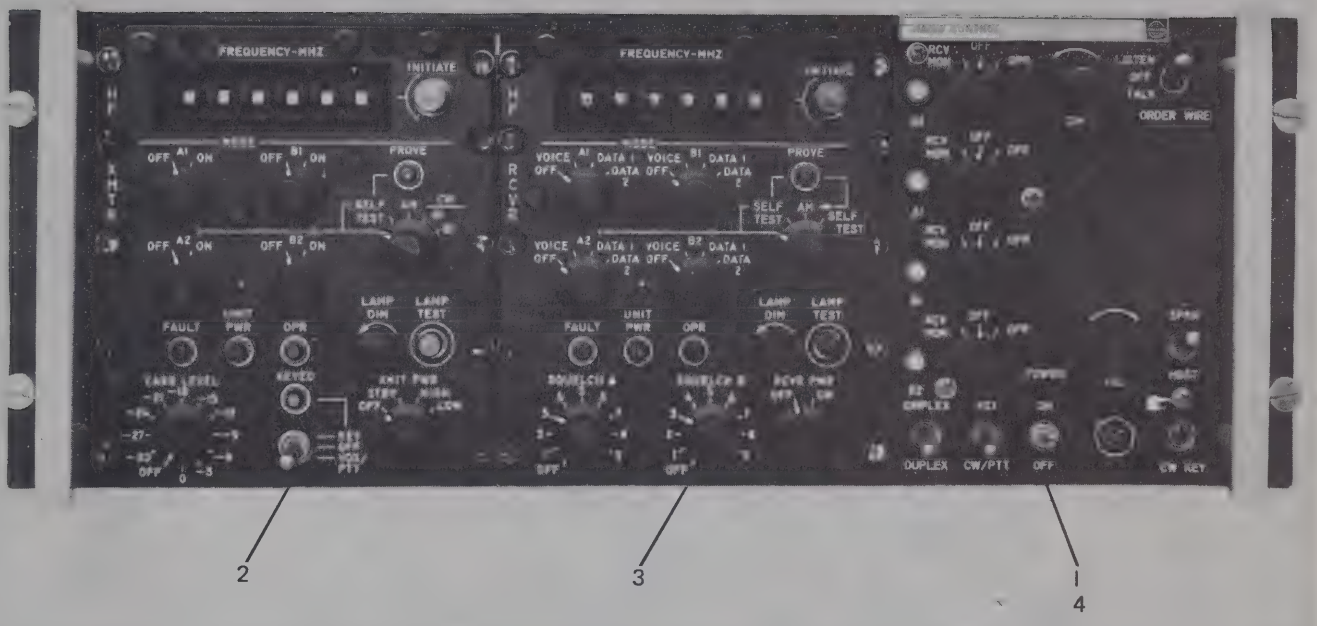
(6) Turn to section II and find the first figure and index number indicated in the Numerical Index for that part. If this figure shows the part in a section or system of the equipment other than the one desired, refer to the other figure numbers listed in the Numerical Index.

(7) On the face of the illustration, find the index number determined in step (6).

(8) If the reference designation symbol is known, refer to section IV to find the part number.

SECTION II

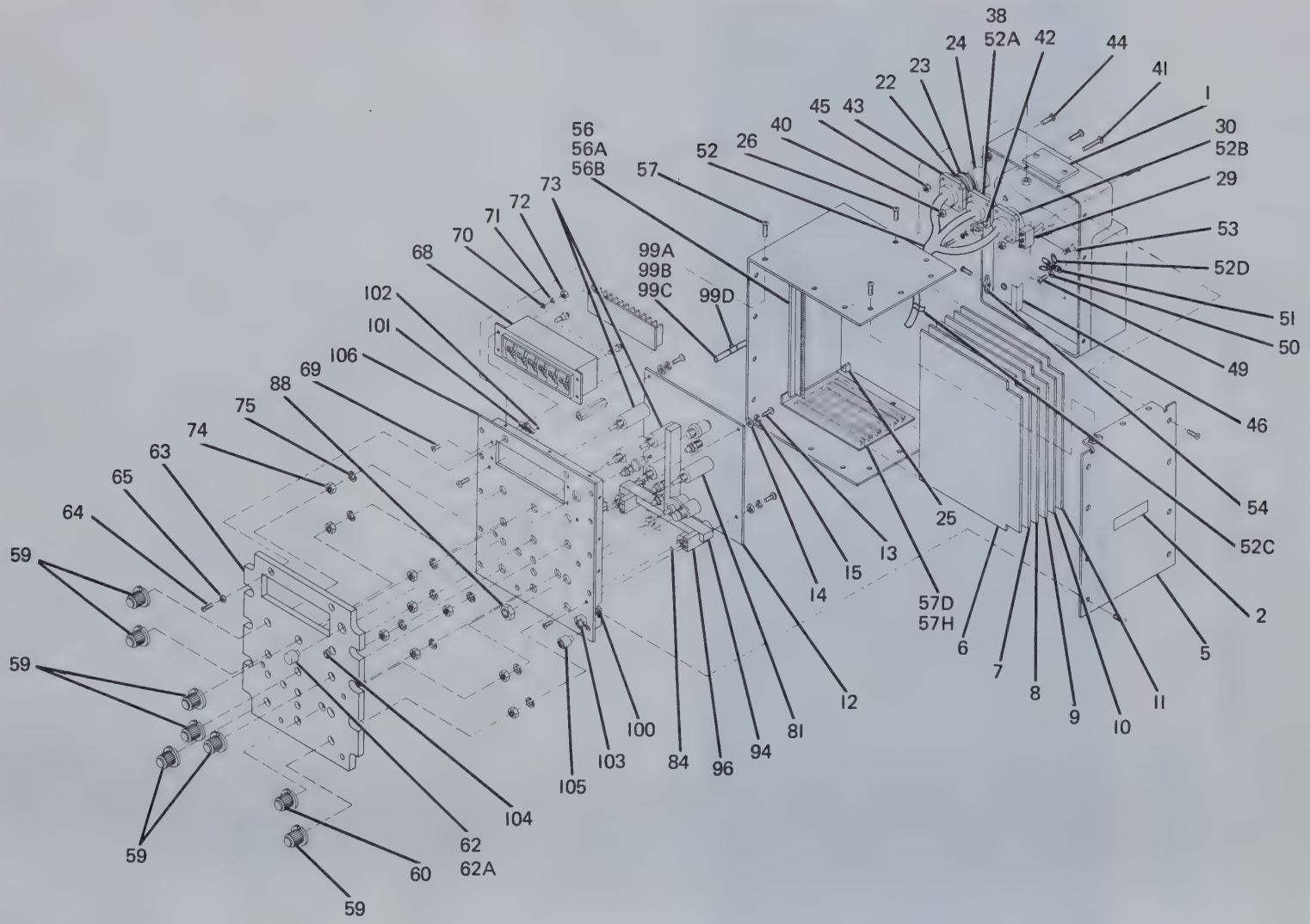
GROUP ASSEMBLY PARTS LIST



B700 2003 Pb

Figure 6-1. Radio Control Group

FIGURE AND INDEX NO.	PART NUMBER	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
1	789-7497-001	RADIO CONTROL GROUP	1	
- 1	795-8763-001	. NAMEPLATE /EFF TO REV LTR B/.	1	
- 1	795-8763-000	. NAMEPLATE /EFF WITH REV LTR B/.	1	
		-ATTACHING PARTS-		
	330-4025-020	. SCREW, TAPPING, SST, 2-56 X 3/16 /45722/ /330-4025-020/	2	
		---*---		
- 2	787-6487-001	. HEAD, TRANSMIT CONTROL C-8363/TSC-60 /V/ /SEE FIGURE 2 FOR. . . BREAKDOWN/	1	
- 3	787-6444-001	. HEAD, RECEIVE CONTROL C-8362/TSC-60 /V/ /SEE FIGURE 13 FOR. . . BREAKDOWN/	1	
- 4	789-8117-001	. UNIT, AUDIO CONTROL C-8364/TSC-60 /V/ /SEE FIGURE 14 FOR. . . . BREAKDOWN/	1	



B700 1052A Bx

Figure 6-2. Transmit Control Head A7 (Sheet 1 of 3)

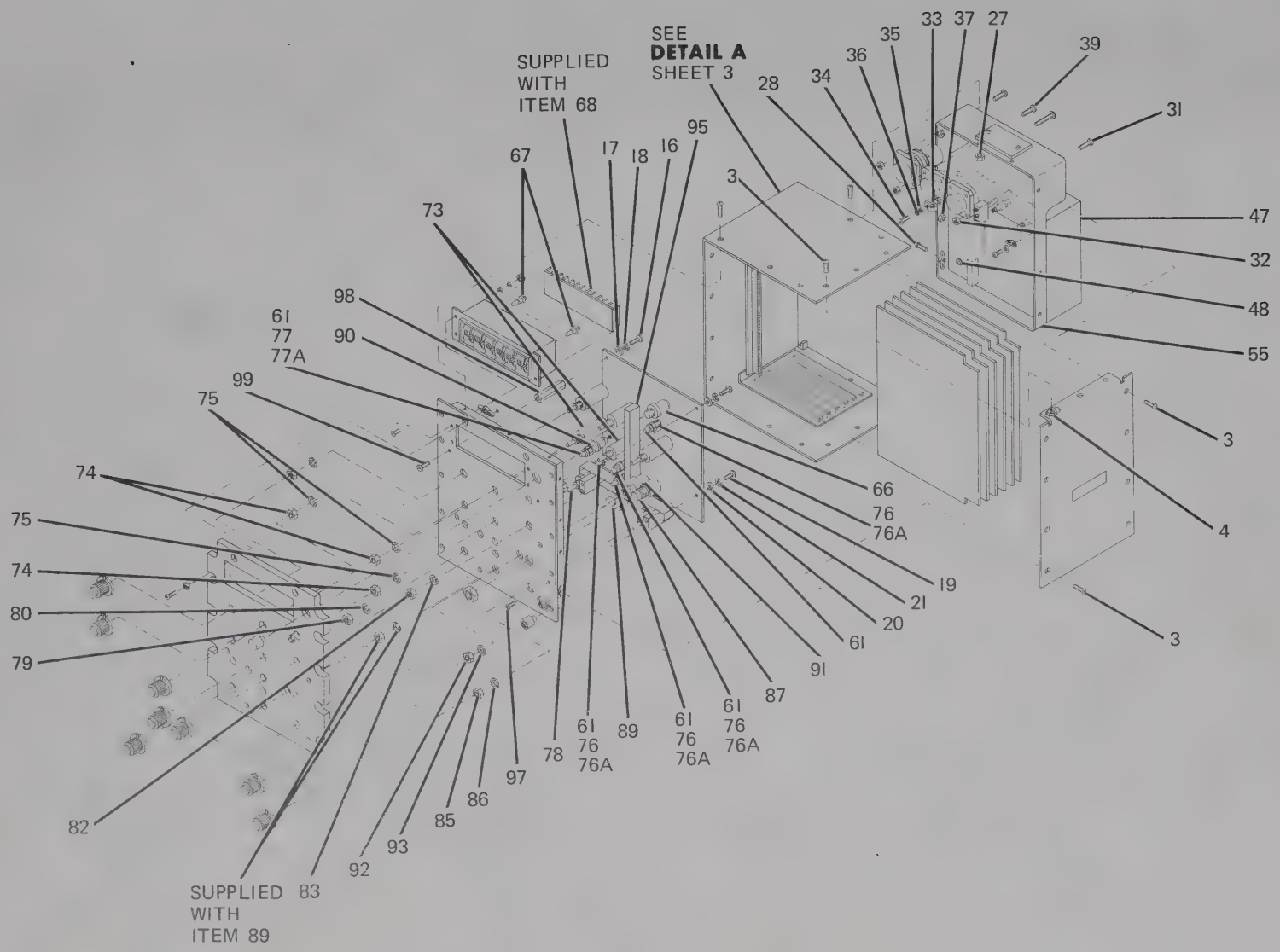
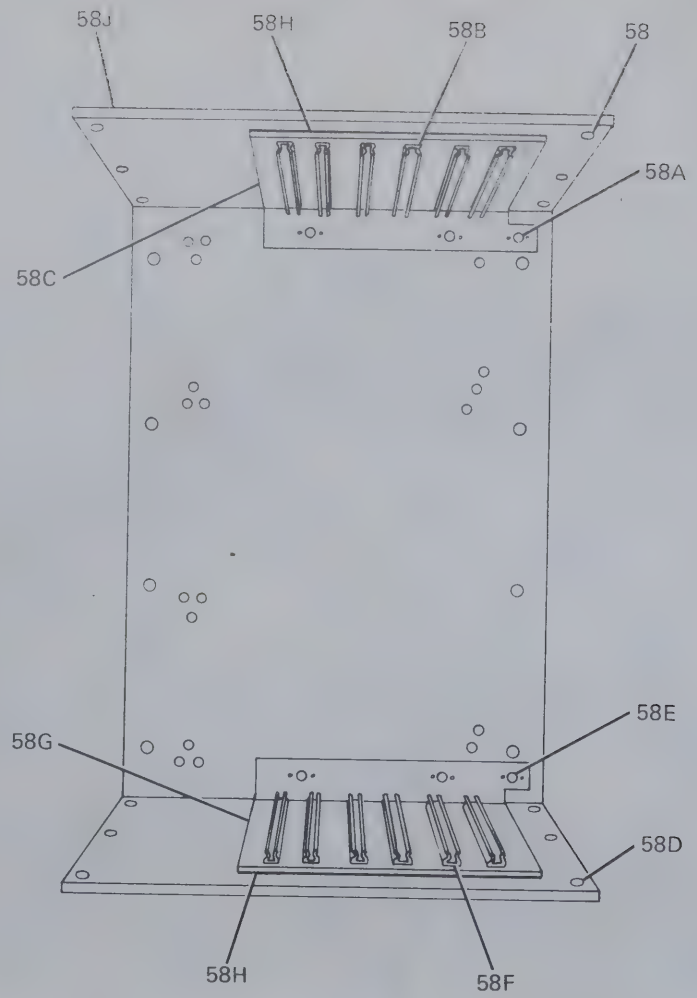


Figure 6-2. Transmit Control Head A7 (Sheet 2 of 3)



B700 2805 Bx

Figure 6-2. Transmit Control Head A7 (Sheet 3 of 3)

FIGURE AND INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
2	787-6487-001	HEAD, TRANSMIT CONTROL C-8363/TSC-60 /V/ /SEE FIGURE 1 FOR NHA/ .	REF	
- 1	795-8765-001	. NAMEPLATE /EFF TO REV LTR W/.	1	
- 1	795-8765-000	. NAMEPLATE /EFF WITH REV LTR W/.	1	
		-ATTACHING PARTS-		
	330-4025-020	. SCREW, TAPPING, SST, 2-56 X 3/16 /45722/ /330-4025-020/	2	
		---*---		
- 2	280-3035-000	. LABEL, INSTRUCTION /16319/ /280-3035-000/ /EFF TO CI-72357/ . .	1	
- 2	280-1339-010	. LABEL, INSTRUCTION /16319/ /280-1339-010/ /EFF WITH CI-72357/ .	1	
	789-2640-001	. COVER, CARD CAGE.	1	
		-ATTACHING PARTS-		
- 3	MS24693C25	. SCREW /342-1350-160/.	12	
		---*---		
- 4	NAS1068A06	. . NUT /333-0888-000/.	6	
- 5	789-2639-002	. . COVER	1	
- 6	793-9260-001	. CARD, LOGIC LEVEL SLAVE /SEE FIGURE 3 FOR BREAKDOWN/.	1	
- 7	789-2620-001	. CARD, HARDWIRE MEMORY /SEE FIGURE 4 FOR BREAKDOWN/ /EFF TO REV. LTR W/	1	
- 7	633-9332-001	. CARD, HARDWIRE MEMORY /SEE FIGURE 4A FOR BREAKDOWN/ /EFF WITH . REV LTR W/	1	
- 8	789-2618-001	. CARD, CCCS TIMING /SEE FIGURE 5 FOR BREAKDOWN/.	1	
- 9	789-2622-001	. CARD, PROCESSOR /SEE FIGURE 6 FOR BREAKDOWN/.	1	
- 10	789-2624-001	. CARD, INSTRUCTION DECODE /SEE FIGURE 7 FOR BREAKDOWN/	1	
- 11	793-8982-001	. CARD, ACCESSIBLE MEMORY /SEE FIGURE 8 FOR BREAKDOWN/.	1	
- 12	789-2612-001	. CARD, MATRIX /SEE FIGURE 9 FOR BREAKDOWN/	1	
		-ATTACHING PARTS-		
- 13	MS51957-14	. SCREW /343-0134-000/.	1	
- 14	DIE845	. WASHER, FLAT, SST, 0.119 ID X 0.218 OD /72606/ /310-0460-000/ .	1	
- 15	310-0278-000	. WASHER, LOCK, SST, 0.115 ID X 0.202 OD /70318/ /310-0278-000/ .	1	
- 16	MS51957-18	. SCREW /343-0138-000/.	2	
- 17	DIE845	. WASHER, FLAT, SST, 0.119 ID X 0.218 OD /72606/ /310-0460-000/ .	2	
- 18	310-0278-000	. WASHER, LOCK, SST, 0.115 ID X 0.202 OD /70318/ /310-0278-000/ .	2	
- 19	MS51957-4	. SCREW /343-0125-000/.	4	
- 20	310-6320-000	. WASHER, FLAT, SST, 0.092 ID X 0.218 OD /79807/ /310-6320-000/ .	4	
- 21	310-0070-000	. WASHER, LOCK, SST, 0.097 ID X 0.165 OD /79807/ /310-0070-000/ .	4	
		---*---		
	795-5244-001	. CONNECTOR, ADDRESS STRAPPING.	1	
- 22	JTG06A14-37P014	. . CONNECTOR, PLUG, ELEC /77820/ /371-9007-110/.	1	
	795-5245-001	. . SHIELD ASSEMBLY	1	
- 23	10-35[illegible]21-14	. . . ADAPTER, THREADED RING /77820/ /371-9006-390/	1	
- 24	789-2667-001	. . . COVER, CONNECTOR.	1	
- 25	789-2666-001	. HOLDDOWN, CONNECTOR	2	
		-ATTACHING PARTS-		
	MS51957-21	. SCREW /343-0141-000/.	2	
	DIE845	. WASHER, FLAT, SST, 0.119 ID X 0.218 OD /72606/ /310-0460-000/ .	2	
		---*---		
	789-2596-001	. PANEL ASSEMBLY, REAR.	1	
		-ATTACHING PARTS-		
- 26	MS24693C24	. SCREW /342-1350-150/.	4	
- 27	P313-0045-000	. NUT, PLAIN, HEX, 6-32 /77250/ /313-0045-000/.	4	
- 28	MS24693C25	. SCREW /342-1350-160/.	4	
		---*---		
- 29	MS75028-23	. . SWITCH /266-5393-030/	1	
- 30	MS27508E16B55P	. . CONNECTOR, RCPT, ELEC /96906/ /359-0609-260/.	1	
		-ATTACHING PARTS-		
- 31	MS51957-15	. . SCREW /343-0135-000/.	4	
- 32	68NM40	. . NUT, SLFLKG, HEX, AL, 4-40 /72962/ /333-0347-000/	4	
		---*---		
- 33	HP8N	. . CLAMP, LOOP /09922/ /150-1545-000/.	1	
		-ATTACHING PARTS-		
- 34	MS51957-14	. . SCREW /343-0134-000/.	1	
- 35	310-6340-000	. . WASHER, FLAT, SST, 0.125 ID X 0.281 OD /79807/ /310-6340-000/	1	
- 36	310-0278-000	. . WASHER, LOCK, SST, 0.115 ID X 0.202 OD /70318/ /310-0278-000/	1	
		---*---		
- 37	540-9176-003	. . POST.	1	
- 38	JTP02RE12-98P014	. . CONNECTOR, RCPT, ELEC /77820/ /359-0609-110/.	1	
		-ATTACHING PARTS-		
- 39	MS51957-15	. . SCREW /343-0135-000/.	3	
- 40	68NM40	. . NUT, SLFLKG, HEX, AL, 4-40 /72962/ /333-0347-000/	3	
- 41	MS51957-16	. . SCREW /343-0136-000/.	1	
- 42	MS35649-244	. . NUT /313-0043-00/	1	
		---*---		
- 43	JTP02RE14-37S014	. . CONNECTOR, RCPT, ELEC /77820/ /359-0607-160/.	1	
		-ATTACHING PARTS-		
- 44	MS51957-15	. . SCREW /343-0135-000/.	4	
- 45	68NM40	. . NUT, SLFLKG, HEX, AL, 4-40 /72962/ /333-0347-000/	4	
		---*---		
- 46	372-2626-045	. . HOUSING, CONNECTOR.	1	
- 47	793-9305-001	. . POWER SUPPLY /SEE FIGURE 10 FOR BREAKDOWN/.	1	
		-ATTACHING PARTS-		
- 48	MS51957-42	. . SCREW /343-0186-000/.	3	
	MS35333-72	. . WASHER /373-0003-000/	3	
- 49	MS51957-43	. . SCREW /343-0187-000/.	1	
- 50	MS35333-72	. . WASHER /373-0003-000/	1	
		---*---		
- 51	2104-08-02-2520N	. . TERMINAL, LUG /78189/ /304-0319-000/.	1	
- 52	795-8757-001	. . CABLE	1	
- 52A	372-2255-010	. . . CONTACT, ELEC	10	
- 52B	372-2255-020	. . . CONTACT, ELEC	59	
- 52C	SSTINAT	. . . STRAP, CABLE /EFF TO REV LTR G/	100	
- 52C	MS3367-4-9	. . . TIE, CABLE /435-1169-100/ /EFF WITH REV LTR G/.	100	

FIGURE AND INDEX NO.	PART NUMBER	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
2 - 52D	CK63AW103M	. . . CAPACITOR/81349/ /913-1188-000/	3	
- 53	TF300	. . TERMINAL, STUD /98291/ /306-1018-000/ . .	3	
		-ATTACHING PARTS-		
	MS51959-1	. . SCREW /342-0131-000/ /EFF TO REV LTR W/ .	3	
	MS51959-2	. . SCREW /342-0132-000/ /EFF WITH REV LTR W/	3	
		---*---		
	789-2660-001	. . PANEL, REAR	1	
- 54	NAS1068A06	. . . NUT, SELFLKG PLATE /72962/ 333-0888-000/	8	
		-ATTACHING PARTS-		
	MS20426AD2-3	. . . RIVET /305-1352-000/	16	
		---*---		
- 55	789-2588-003	. . . PANEL, REAR, FABRICATED	1	
	789-2626-001	. CARD, BACKPLANE	1	
		-ATTACHING PARTS-		
	MS51957-14	. . SCREW /343-0134-000/ /EFF TO REV LTR Z/ .	4	
	MS51957-15	. SCREW /343-0135-000/ /EFF WITH REV LTR Z/ .	4	
	302-4800-000	. WASHER, NM FBR, 0.116 ID X 1/4 OD /74921/ .	4	
		/302-4800-000/ /EFF WITH REV LTR Z/		
	DIE845	. WASHER, FLAT, SST, 0.199 ID X 0.218 OD /72606/	4	
		/310-0460-000/ ---*---		
- 56	768-5919-003	. . PIN POLARIZING		
- 57	MS20426AD2-4	. . RIVET /305-1353-000/	9	
- 56A	372-2601-045	. . CONTACT, ELEC		
- 57A	LHTA57M2860-40	. . . NUT PLATE, 4-40 /72962/ /333-1449-010/.	3	
- 56B	600-9276-011	. . BACKPLANE, FAB		
	789-2592-001	. CAGE, CARD.	1	
		-ATTACHING PARTS-		
- 57	MS24693C25	. SCREW /342-1350-160/.	10	
		---*---		
	789-2657-001	. . GUIDE ASSEMBLY, UPPER	1	
		-ATTACHING PARTS-	1	
- 58	MS20426AD2-4	. . RIVET /305-1353-000/	9	
		---*---		
- 58A	LHTA57M2860-40	. . . NUT PLATE, 4-43 /72962/ /333-1449-010/.	3	
		-ATTACHING PARTS-		
	MS20426AD2-3	. . . RIVET /305-1352-000/.	6	
		---*---		
- 58B	775-466C-007	. . . GUIDE CARD, GRIP.	6	
- 58C	789-2656-001	. . . GUIDE, PLATE.	1	
	789-2636-001	. . GUIDE ASSEMBLY, LOWER	1	
		-ATTACHING PARTS-		
- 58D	MS20426AD2-4	. . RIVET /305-1353-000/.	9	
		---*---		
- 58E	LHTA57M2860-40	. . . NUT PLATE, 4-40 /72962/ 333-1449-010/ .	3	
		-ATTACHING PARTS-		
	MS20426AD2-3	. . . RIVET /305-1352-000/.	6	
		---*---		
- 58F	775-466C-007	. . . GUIDE CARD, GRIP.	6	
- 58G	789-2597-001	. . . GUIDE, PLATE.	1	
- 58H	795-5246-001	. . SHIELD, KNITTED MESH	2	

FIGURE AND INDEX NO.	PART NUMBER	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
- 58J	789-2641-001	. . FRAME, CARD CAGE.	1	
- 59	MS91528-OH1B	. KNOB /281-0188-040/	7	
- 60	MS91528-001B	. KNOB /281-0386-0007//EFF WITH REV LTR Y/ . . .	1	
	633-4570-001	. KNOB /EFF WITH REV LTR Y/	1	
- 61	MS24515-685	. LAMP, INCANDESCENT /17537/ /262-2204-060/ . . .	5	
- 62	381	. LAMP, INCANDESCENT /24455/ /262-2113-000/ . . .	1	
- 62A	183-1474-001	. . LENS, CAP /72619/	1	
- 63	789-2584-005	. PANEL, ILLUMINATED.	1	
		-ATTACHING PARTS-		
- 64	P343-0035-000	. SCREW, MACH, SST, 6-32 X 7/16 /77250/ . . . . . /343-0035-000/	6	
- 65	759-4321-001	. WASHER, SHOCK /EFF TO C1 73037/	6	
	5610-59-32	. WASHER, NON-METALLIC, 0.114 ID X 0.270 OD . . . /86928/ EFF WITH C1-73037/	6	
		---*---		
	789-2594-001	. PANEL ASSEMBLY, FRONT	1	
- 66	183-0101-1474-60	. . SWITCH, PUSH /72619/ /266-7086-170/	1	
- 67	MS24515-685	. . LAMP, INCADESCENT /17537/ /262-2204-060/. . .	6	
- 68	7C38	. . SWITCH, RTRY /07125/ /259-9590-030/	1	
		-ATTACHING PARTS-		
- 69	MS51959-3	. . SCREW /342-0133-000/ /EFF TO REV LTR W/ . . .	4	
	MS51959-4	. . SCREW /342-0134-000/ /EFF WITH REV LTR W/ . .	4	
- 70	310-6320-000	. . WASHER, FLAT, SST, 0.092 ID X 0.218 OD. . . . /79807/ /310-6320-000/	4	
- 71	310-0070-000	. . WASHER, LOCK, SST, 0.097 ID X 0.165 OD. . . . /79807/ /310-0070-000/	4	
- 72	MS35649-224	. . NUT /313-0037-000/.	4	
		---*---		
- 73	259-27669-010	. . SWITCH, RTRY.	4	
		-ATTACHING PARTS-		
- 74	P334-0287-00	. . NUT, PLAIN, HEX, SST, 1/4-32 /77250/. . . . . /334-0287-000/	4	
- 75	1214-05CDPL	. . WASHER, LOCK, STL, 0.267 ID X 0.408 OD . . . /78189/ /373-0151-000/	4	
		---*---		
- 76	5160-458-604GRN	. . LIGHT IND /72765/ /262-2322-060/.	4	
- 76A	160A604GRN	. . . LENS /72765/ /262-2322-130/	4	
- 77	5160-458-604RED	. . LIGHT, IND /72765/ /262-2322-070/	1	
- 77A	160A604RED	. . . LENS /72765/ /262-2322-140/	1	
- 78	259-2769-030	. . SWITCH, RTRY.	1	
		-ATTACHING PARTS-		
- 79	P334-0287-00	. . NUT, PLAIN, HEX, SST, 1/4-32 /77250/. . . . . /334-0287-000/	1	
- 80	1214-05CDPL	. . WASHER, LOCK, STL, 0.267 ID X 0.408 OD. . . . /78189/ /373-0151-000/	1	
		---*---		
- 81	259-2769-090	. . SWITCH, RTRY.	1	

FIGURE AND INDEX NO.	PART NUMBER	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
2		-ATTACHING PARTS-		
- 82	P334-0287-00	. . NUT, PLAIN, HEX, SST, 1/4-32 /77250/ /334-0287-000/	1	
- 83	1214-05CDPL	. . WASHER, LOCK, STL, 0.267 ID X 0.408 OD /78189/ /373-0151-000/	1	
		---*---		
- 84	259-2769-050	. . SWITCH, RTRY.	1	
		-ATTACHING PARTS-		
- 85	P334-0287-00	. . NUT, PLAIN, HEX, SST, 1/4-32 /77250/ /334-0287-000/	1	
- 86	1214-05CDPL	. . WASHER, LOCK, STL, 0.267 ID X 0.408 OD /78189/ /373-0151-000/	1	
		---*---		
- 87	W1046	. . SWITCH, PUSH /81640/ /266-2701-020/ /EFF TO REV LTR W/. . . .	1	
- 87	W1046CE	. . SWITCH, PUSH /81640/ /266-2701-060/ /EFF WITH REV LTR W/. . .	1	
		-ATTACHING PARTS-		
- 88	318-0035	. . NUT, PLAIN, RD, BRS, 1/2-32 /97564/ /334-2736-020/.	1	
		/EFF WITH REV LTR W/		
- 88		DELETED /EFF WITH REV LTR W/		
		---*---		
- 89	MS90311-211	. . SWITCH /266-5193-000/	1	
- 90	130GOLD	. . CONNECTOR, RCPT, ELEC /04211/ /372-2225-010/.	1	
- 91	M22-01-00091SB	. . RESISTOR /749-4727-030/	1	
		-ATTACHING PARTS-		
- 92	P334-0287-00	. . NUT, PLAIN, HEX, SST, 1/4-32 /77250/ /334-0287-000/	1	
		/EFF TO REV LTR M/		
- 92		DELETED /EFF WITH REV LTR M/		
- 93	1214-05CDPL	. . WASHER, LOCK, STL, 0.267 ID X 0.408 OD /78189/ /373-0151-000/	1	
		---*---		
- 94	789-2652-001	. . CONNECTOR, NO. 1.	1	
		-ATTACHING PARTS-		
	MS51957-9	. . SCREW /343-0129-000/.	2	
	310-6320-000	. . WASHER, FLAT, SST, 0.092 ID X 0.218 OD /79807/ /310-6320-000/	2	
	68NM26	. . NUT, SLFLKG, HEX, AL, 2-56 /72962/ /333-0327-000/	2	
		---*---		
- 95	789-2653-001	. . CONNECTOR, NO. 2.	1	
		-ATTACHING PARTS-		
	MS51957-9	. . SCREW /343-0129-000/.	2	
	310-6320-000	. . WASHER, FLAT, SST, 0.092 ID X 0.218 OD /79807/ /310-6320-000/	2	
	68NM26	. . NUT, SLFLKG, HEX, AL, 2-56 /72962/ /333-0327-000/	2	
		---*---		
- 96	789-2590-001	. . POST, CONNECTOR MOUNTING.	4	
		-ATTACHING PARTS-		
- 97	MS51959-14	. . SCREW /342-0045-000/.	8	
		---*---		
- 98	789-2637-001	. . POST, HEX	3	
		-ATTACHING PARTS-		
- 99	MS51959-14	. . SCREW /342-0045-000/.	3	
		---*---		
- 99A	795-8756-001	. . CABLE, FRONT PANEL.	1	
- 99B	372-2255-020	. . . CONTACT, ELEC	47	
- 99C	372-2255-010	. . . CONTACT, ELEC	10	
- 99D	SSTINAT	. . . STRAP, CABLE /06383/ /150-0681-050/ /EFF TO REV LTR L/. . .	100	
- 99D	MS3367-4-9	. . . TIE, CABLE /435-1169-100/ /EFF WITH REV LTR L/-	100	
	789-2589-001	. . PANEL, FABRICATED	1	
		PARTIAL BREAKDOWN FOLLOWS		
-100	NAS1068A06	. . . NUT PLATE /333-0888-000/.	14	
		-ATTACHING PARTS-		
	MS20426AD2-3	. . . RIVET /305-1352-000/.	28	
		---*---		
-101	LHTA51M2860-62	. . . NUT PLATE, SLFLKG, SST, 6-32 /72962/ /333-1157-000/	2	
		-ATTACHING PARTS-		
-102	MS20426AD2-3	. . . RIVET /305-1352-000/.	4	
		---*---		
-103	MRPN6-32SCL	. . . NUT, PRSD, CD PL STL, 6-32 /83324/ /334-2615-000/	4	
-104	793-6249-001	. . . BUSHING, INDICATOR LIGHT.	5	
-105	PFSC3 1-2 38	. . . STUD ASSY /72794/ /012-0003-010/.	10	
-106	789-2680-001	. . . PANEL, FABRICATED	1	

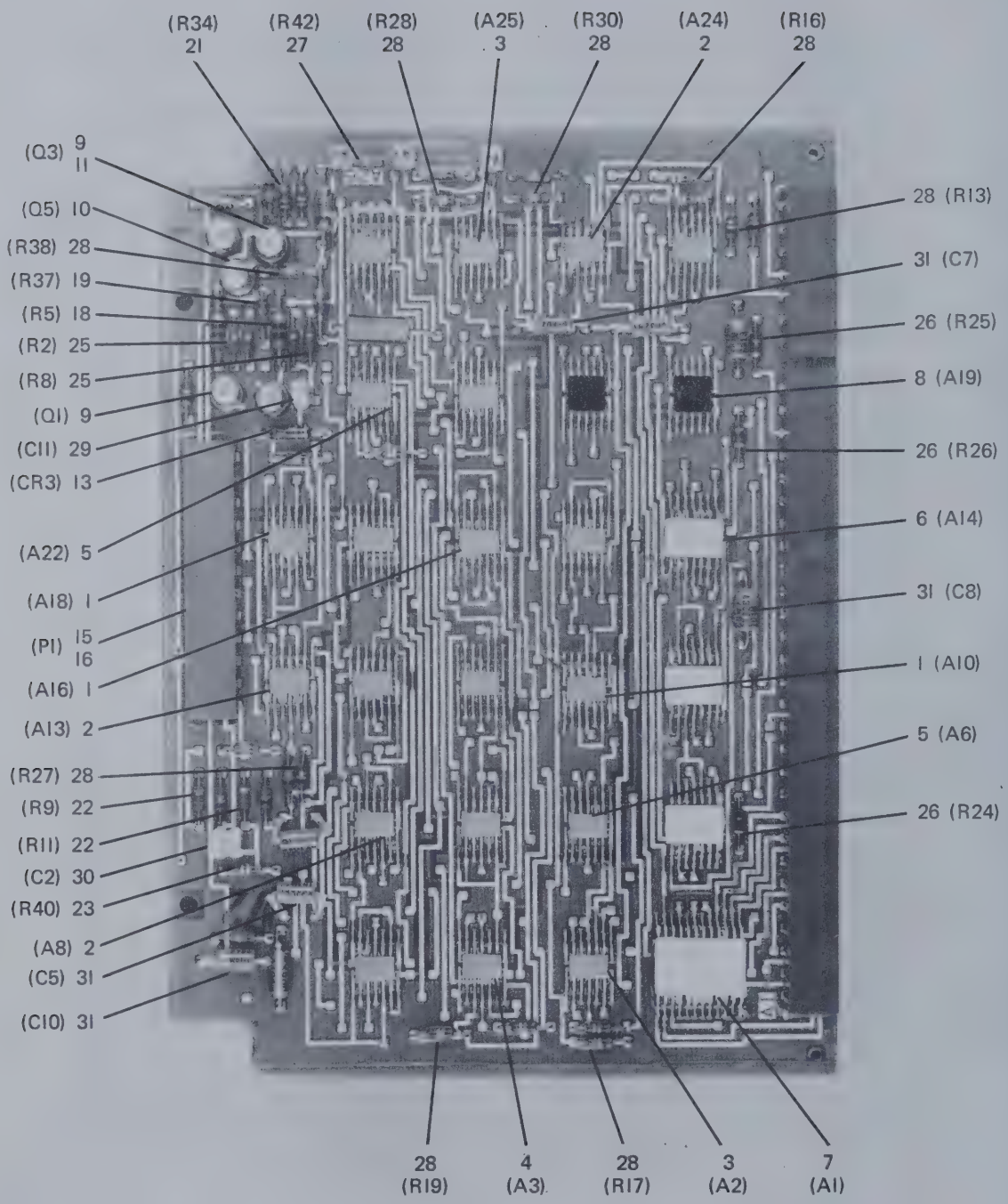


Figure 6-3. Logic Level Slave Card A7A1, A8A1 (Sheet 1 of 2)

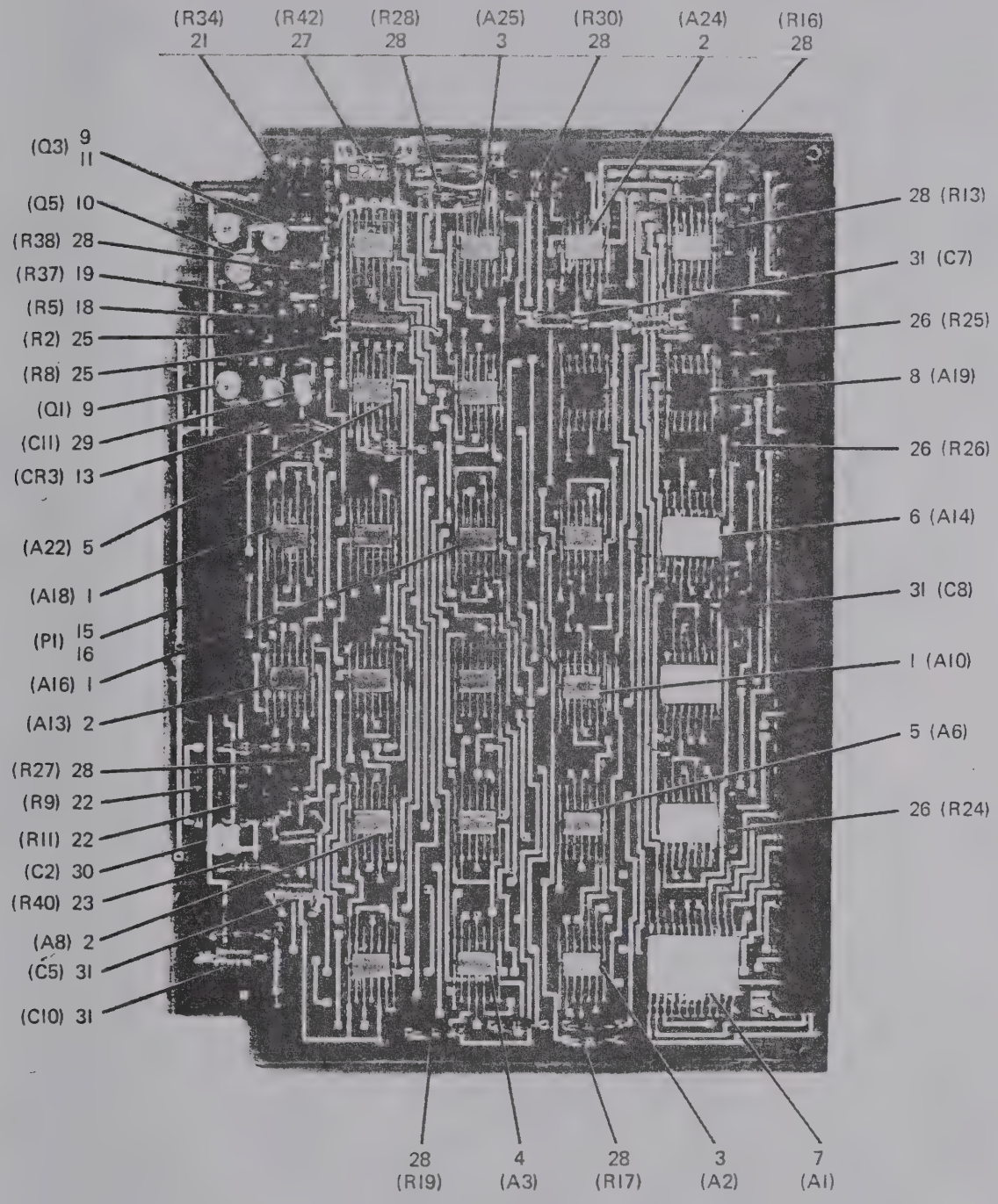


Figure 6-3. Logic Level Slave Card A7A1, A8A1 (Sheet 2 of 2)

FIGURE AND INDEX NO.	PART NUMBER	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
3	793-9260-001	CARD, LOGIC LEVEL SLAVE /SEE FIGURES 2 AND 13 FOR NHA/.	REF	
- 1	54L00SD7722A	. INTEGRATED CIRCUIT /12040/ /351-7365-012/	10	
- 2	54L10SD7723A	. INTEGRATED CIRCUIT /12040/ /351-7365-022/	3	
- 3	54L20SD7724A	. INTEGRATED CIRCUIT /12040/ /351-7365-032/	2	
- 4	54L73SD9545A	. INTEGRATED CIRCUIT /12040/ /351-7365-102/	1	
- 5	SD9857A	. INTEGRATED CIRCUIT /27014/ /351-7390-012/	4	
- 6	UD4225	. INTEGRATED CIRCUIT /13606/ /351-7406-010/	3	
- 7	351-7437-012	. INTEGRATED CIRCUIT.	1	
- 8	351-7445-012	. INTEGRATED CIRCUIT.	2	
- 9	352-7500-191	. TRANSISTOR.	3	
- 10	352-7500-281	. TRANSISTOR.	2	
- 11	7717-130DAP	. INSULATOR, DISK /13103/ /352-9552-580/.	5	
- 12	353-2978-001	. DIODE	1	
- 13	353-3338-001	. DIODE	2	
- 14	372-2623-045	. CONNECTOR, CONTACT.	1	
- 15	372-2621-021	. CONNECTOR, CONTACT.	1	
- 16	372-2234-010	. CONTACT, ELECT.	48	
- 17	372-2234-020	. CONTACT, ELECT.	35	
- 18	RCR07G100KS	. RESISTOR /745-0677-000/	2	
- 19	RCR05G272JS	. RESISTOR /745-1863-590/	1	
- 20	RCR05G332JS	. RESISTOR /745-1863-610/	1	
- 21	RCR05G432JS	. RESISTOR /745-1863-640/	1	
- 21A	RCR05G512JS	. RESISTOR /745-1863-660/	1	
- 22	RCR05G682JS	. RESISTOR /745-1863-690/	2	
- 23	RCR05G103JS	. RESISTOR /745-1863-730/	2	
- 24	RCR05G102K	. RESISTOR /745-2341-000/	2	
- 25	RCR05G222K	. RESISTOR /745-2353-000/	4	
- 26	RCR05G472K	. RESISTOR /745-2365-000/	3	
- 27	RCR05G822K	. RESISTOR /745-2374-000/	1	
- 28	RCR05G103K	. RESISTOR /745-2377-000/	20	
- 29	C5443X152M	. CAPACITOR, FXD, CER, 1500PF, 20%, 50V /96733/ /913-3244-270/. .	1	
- 30	CK073X221K	. CAPACITOR /913-3287-120/.	2	
- 31	CK328V104M	. CAPACITOR /913-4500-700/.	7	
- 32	M39003-01-2117	. CAPACITOR /184-9084-440/.	1	
- 33	M39003-01-2271	. CAPACITOR /184-9086-310/.	1	
- 34	600-0044-007	. BOARD	1	

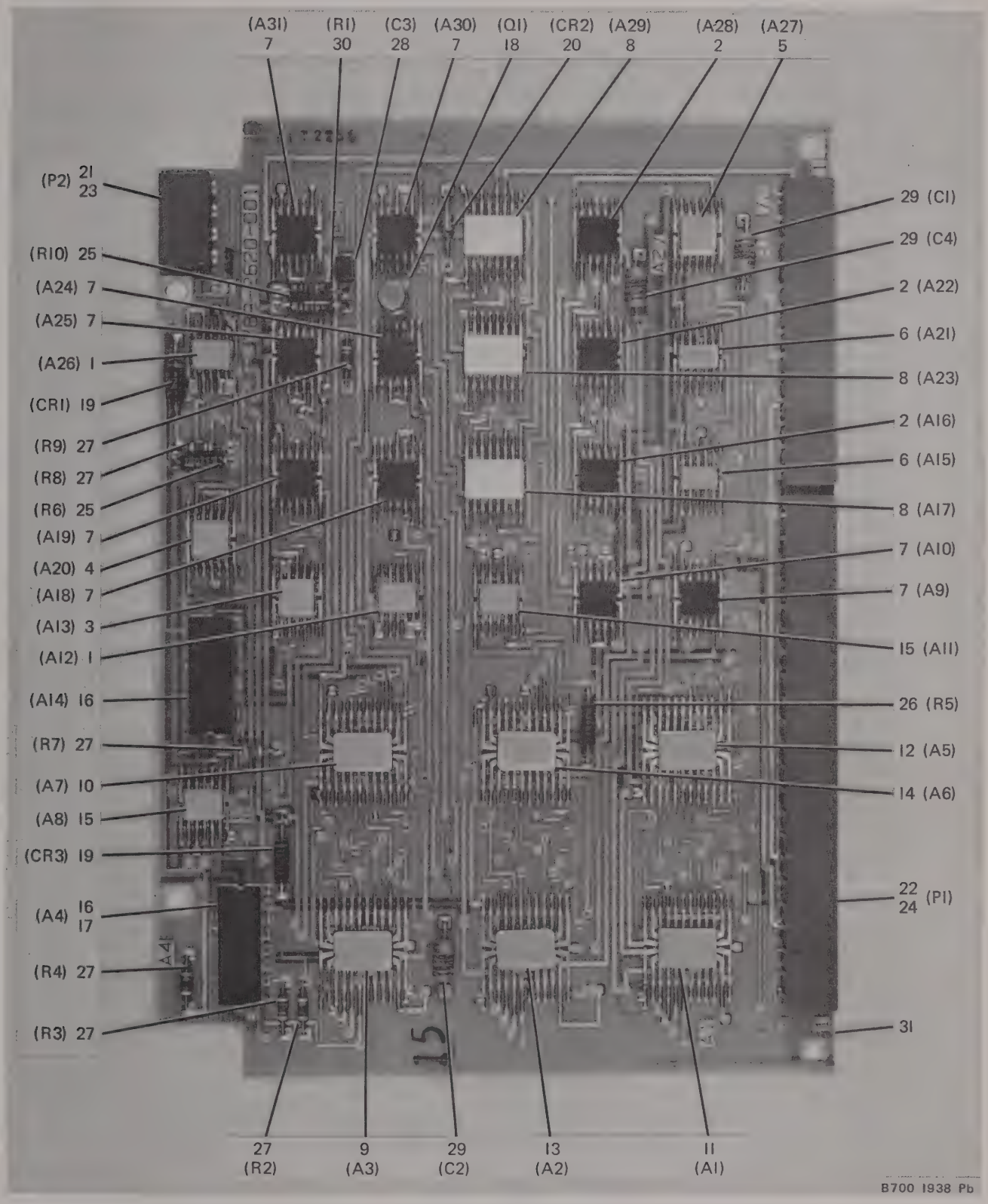
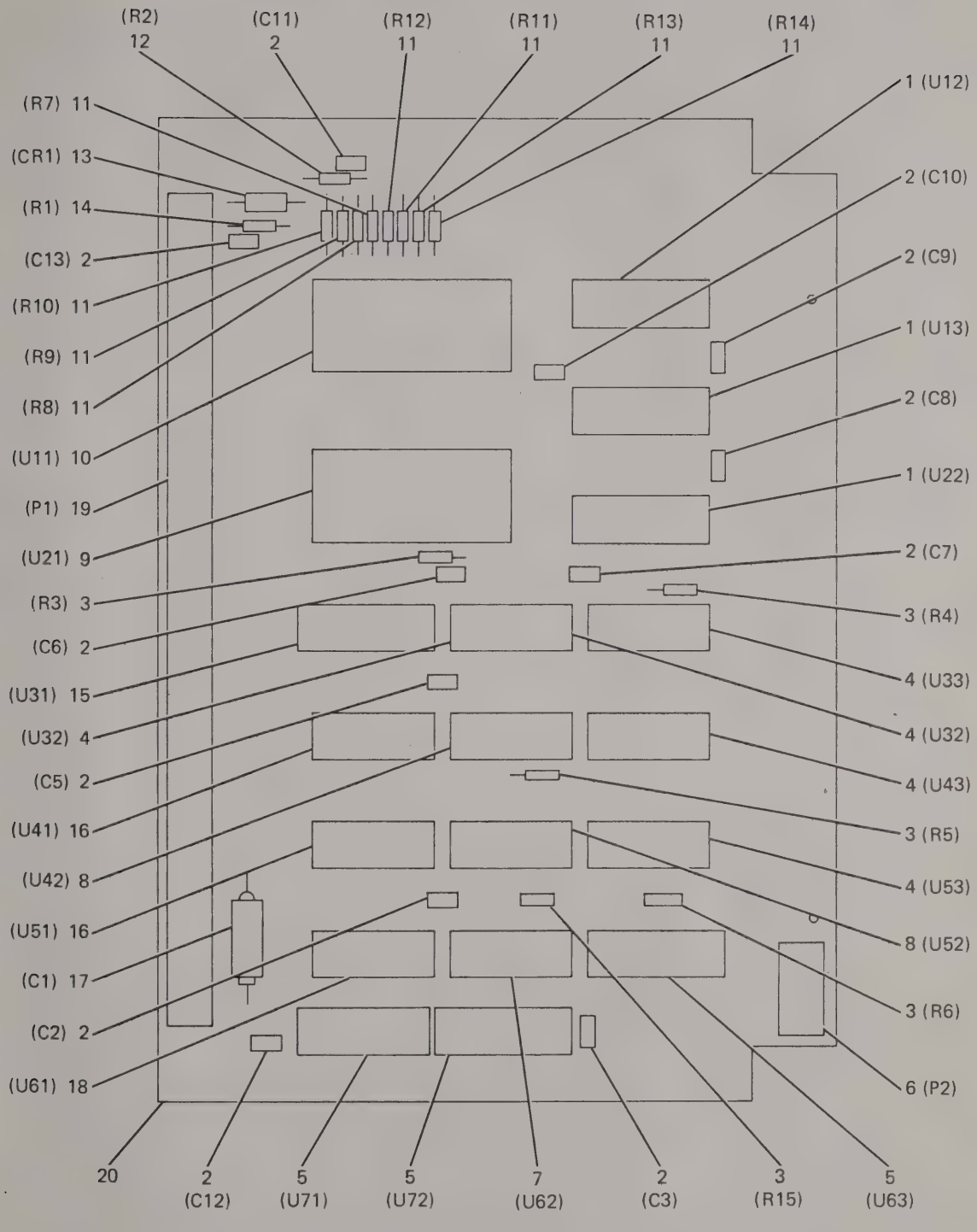


Figure 6-4. Hardwire Memory Card A7A2

FIGURE AND INDEX NO.	PART NUMBER	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
4	789-2620-001	CARD, HARDWIRE MEMORY /SEE FIGURE 2 FOR NHA/ /EFF TO REV LTR W/ .	REF	
- 1	F51K2	. INTEGRATED CIRCUIT /49956/ /351-7107-022/	2	
- 2	SS314	. INTEGRATED CIRCUIT /93332/ /351-7333-022/	3	
- 3	54L00SD7722A	. INTEGRATED CIRCUIT /12040/ /351-7365-012/	1	
- 4	54L20SD7724A	. INTEGRATED CIRCUIT /12040/ /351-7365-032/	1	
- 5	SD9857A	. INTEGRATED CIRCUIT /27014/ /351-7390-012/	1	
- 6	SN19670	. INTEGRATED CIRCUIT /01295/ /351-7401-012/	2	
- 7	HL11561	. INTEGRATED CIRCUIT /07263/ /351-7428-012/	8	
- 8	351-7436-012	. INTEGRATED CIRCUIT.	3	
- 9	H10004S	. INTEGRATED CIRCUIT /14936/ /351-7451-052/	1	
- 10	H10005S	. INTEGRATED CIRCUIT /14936/ /351-7451-062/	1	
- 11	H08014S	. INTEGRATED CIRCUIT /14936/ /351-7451-072/	1	
- 12	H08015S	. INTEGRATED CIRCUIT /14936/ /351-7451-082/	1	
- 13	H12014S	. INTEGRATED CIRCUIT /14936/ /351-7451-092/	1	
- 14	H12015S	. INTEGRATED CIRCUIT /14936/ /351-7451-102/	1	
- 15	G371K2	. INTEGRATED CIRCUIT /07933/ /351-7495-022/	2	
- 16	HL30110	. INTEGRATED CIRCUIT /07263/ /351-8050-012/	2	
- 17	767-1421-001	. PEDESTAL, INTEGRATED CIRCUIT.	31	
- 18	352-7500-281	. TRANSISTOR.	1	
- 19	353-2978-001	. DIODE	2	
- 20	353-3338-001	. DIODE	1	
- 21	372-2621-013	. CONNECTOR, CONTACT.	1	
- 22	372-2623-045	. CONNECTOR, CONTACT.	1	
- 23	372-2234-010	. CONTACT, ELEC	39	
- 24	372-2234-020	. CONTACT, ELEC	35	
- 25	RNR55J1002FM	. RESISTOR /705-1499-010/	2	
- 26	RNR55J2492FM	. RESISTOR /705-1499-390/	1	
- 27	RCR05G472K	. RESISTOR /745-2365-000/	6	
- 28	G544BX182J	. CAPACITOR, FXD, CER, DIEL, 1800PF, 5(TOL, 50V /96733/. . . . . /913-3244-690/	1	
- 29	CK32BV104M	. CAPACITOR /913-4500-700/.	3	
- 30	RNR55J2611FM	. RESISTOR /705-3502-410/	1	
- 31	600-9283-012	. BOARD	1	



B700 3291 Bx

Figure 6-4A. Hardwire Memory Card

FIGURE AND INDEX NO.	PART NUMBER	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
4A	633-9332-001	CARD, HARDWIRE MEMORY /SEE FIGURE 2 FOR NHA/ /EFF WITH REV LTR W/	REF	
- 1	SNC54LS161J	. INTEGRATED CIRCUIT /01295/ /351-1734-010/	3	
- 2	CKR05BX104MM	. CAPACITOR /81349/ /913-9011-360/	12	
- 3	RCR05G102KS	. RESISTOR /81349/ /81349/ /745-2341-000/	5	
- 4	351-1605-011	. INTEGRATED CIRCUIT	4	
- 5	SNC54LS76J	. INTEGRATED CIRCUIT /01295/ /351-1733-010/	3	
- 6	372-2621-013	. CONNECTOR	1	
- 7	M38510-02004BCB	. INTEGRATED CIRCUIT /81349/ /351-7900-150/	1	
- 8	SNC54LS91J	. INTEGRATED CIRCUIT /01295/ /351-1735-010/	2	
- 9	AM27S80DMB0036	. INTEGRATED CIRCUIT /34335/ /351-1718-010/	1	
- 10	AM25S80DMB0037	. INTEGRATED CIRCUIT /34335/ /351-1718-020/	1	
- 11	RCR05G103KS	. RESISTOR /81349/ /745-2377-000/	8	
- 12	RCR05G102JS	. RESISTOR /81349/ /745-1863-730/	1	
- 13	353-2850-001	. DIODE	1	
- 14	RCR05G223JS	. RESISTOR /81349/ /745-1863-810/	1	
- 15	SNC54LS251J	. INTEGRATED CIRCUIT /01295/ /351-1530-080	1	
- 16	351-1523-032	. INTEGRATED CIRCUIT	2	
- 17	M39003-01-2296	. CAPACITOR /81349/ /184-9086-500/	1	
- 18	M38510-02002BCB	. INTEGRATED CIRCUIT /81349/ /351-7900-180/	1	
- 19	372-2623-045	. CONNECTOR	1	
- 20	600-3990-401	. BOARD	1	

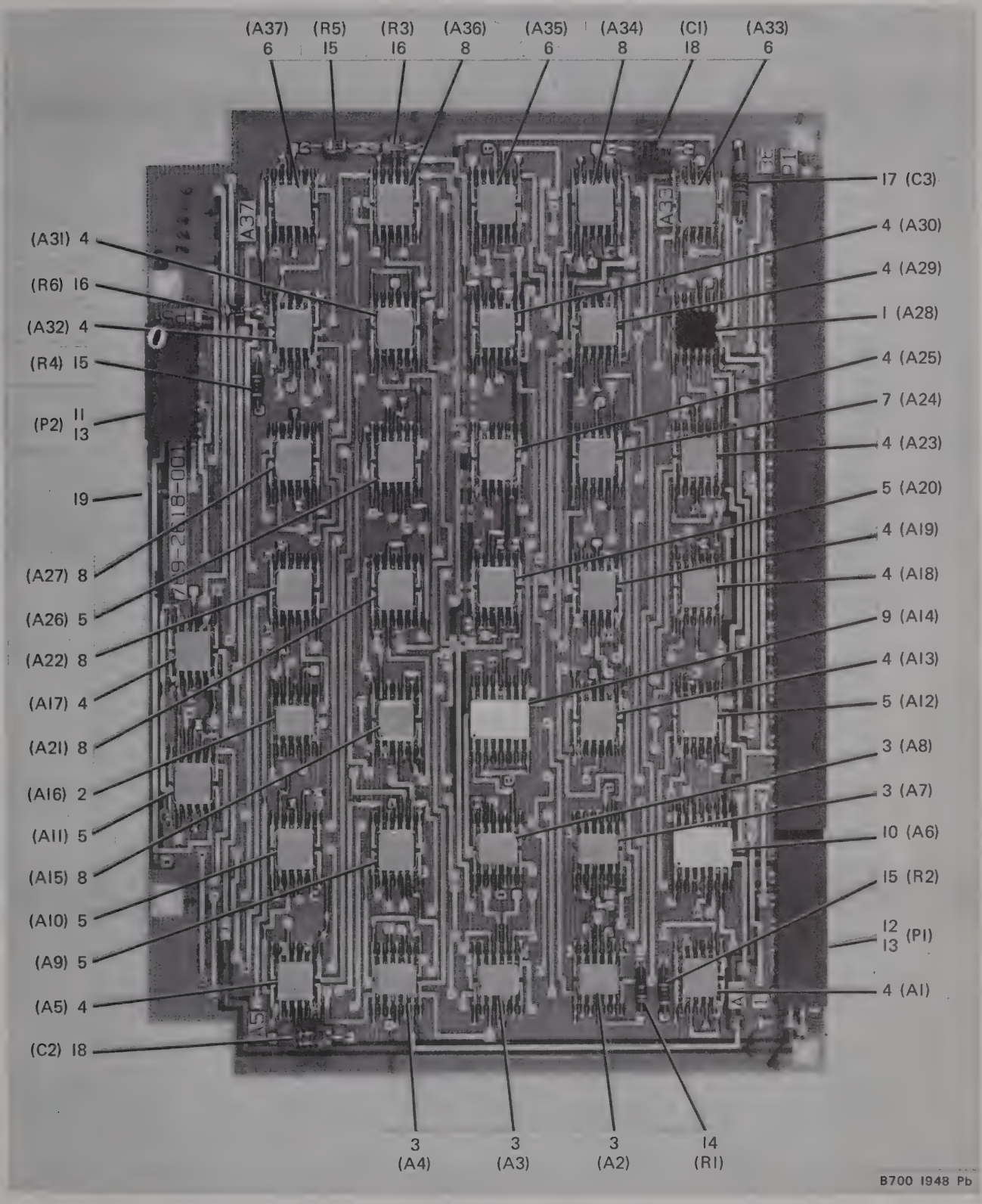


Figure 6-5. CCCS Timing Card A7A3

FIGURE AND INDEX NO.	PART NUMBER	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
5	789-2618-001	CARD, CCCS TIMING /SEE FIGURE 2 FOR NHA/.	REF	
- 1	G191K2	. INTEGRATED CIRCUIT /49956/ /351-7101-022/	1	
- 2	F51K2	. INTEGRATED CIRCUIT /49956/ /351-7107-022/	1	
- 3	SF10112	. INTEGRATED CIRCUIT /93332/ /351-7297-022/	5	
- 4	54L00SD7722A	. INTEGRATED CIRCUIT /12040/ /351-7365-012/	12	
- 5	54L10SD7723A	. INTEGRATED CIRCUIT /12040/ /351-7365-022/	6	
- 6	54L20SD7724A	. INTEGRATED CIRCUIT /12040/ /351-7365-032/	3	
- 7	54L30SD7725A	. INTEGRATED CIRCUIT /12040/ /351-7365-042/	1	
- 8	54L73SD8545A	. INTEGRATED CIRCUIT /12040/ /351-7365-102/	6	
- 9	12397-93015L	. INTEGRATED CIRCUIT /07263/ /351-7386-022/	1	
- 10	HL11554	. INTEGRATED CIRCUIT /07263/ /351-7430-012/	1	
- 11	372-2621-014	. CONNECTOR, CONTACT.	1	
- 12	372-2621-045	. HOUSING, CONN	1	
- 13	372-2234-010	. CONTACT, ELEC	40	
- 14	RCR05G331K	. RESISTOR /745-2323-000/	1	
- 15	RCR05G471K	. RESISTOR /745-2329-000/	3	
- 16	RCR05G821K	. RESISTOR /745-2338-000/	2	
- 17	CK31BT102K	. CAPACITOR /913-4500-010/.	1	
- 18	CK32BV104M	. CAPACITOR /913-4500-700/.	2	
- 19	600-9284-007	. BOARD	1	

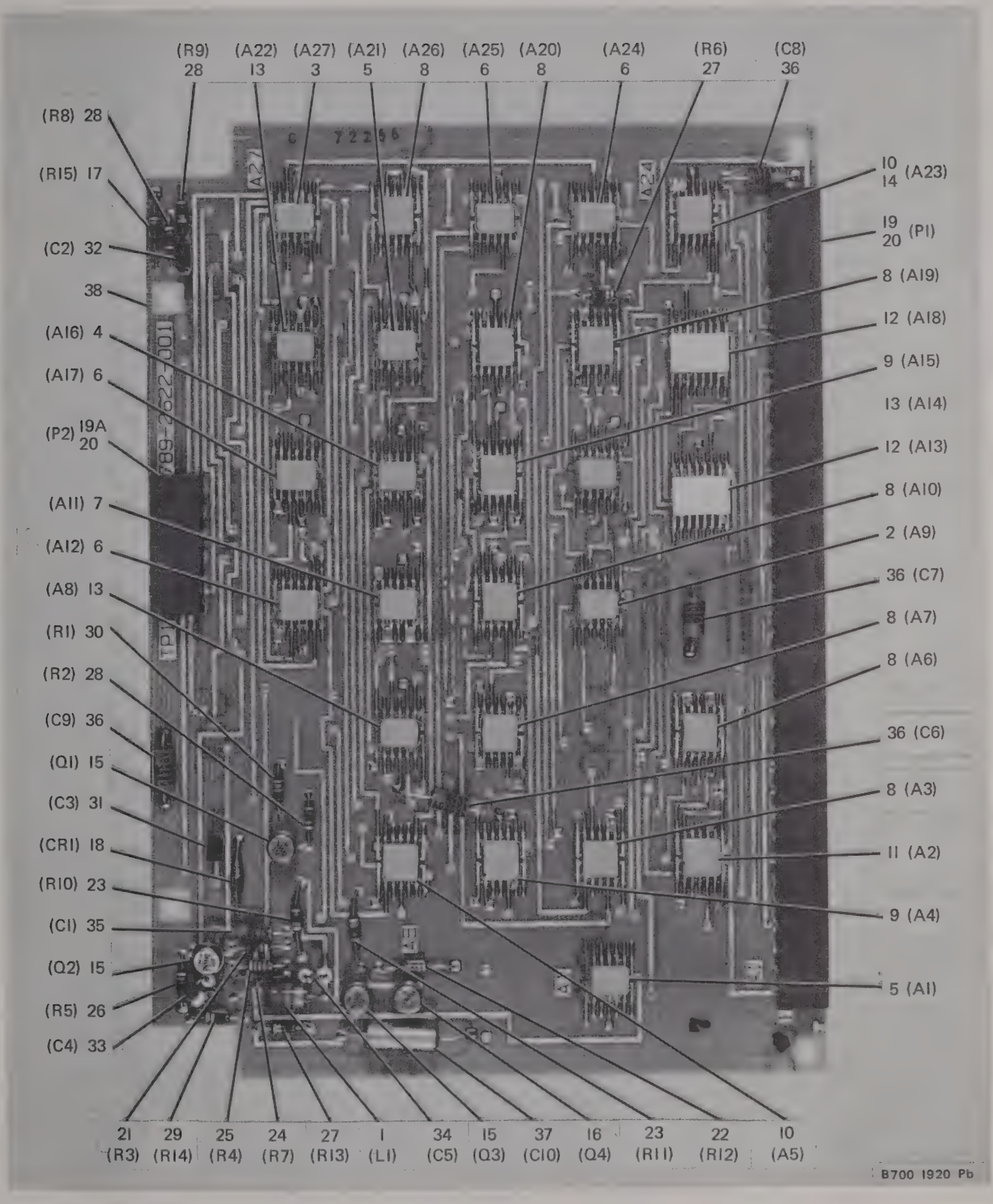


Figure 6-6. Processor Card A7A4

FIGURE AND INDEX NO.	PART NUMBER	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
6	789-2622-001	CARD, PROCESSOR /SEE FIGURE 2 FOR NHA/.	REF	
- 1	MS90537-45	. COIL /240-2715-450/	1	
- 2	G140K2	. INTEGRATED CIRCUIT /49956/ /351-7093-012/	1	
- 3	SG14127	. INTEGRATED CIRCUIT /93332/ /351-7093-022/	1	
- 4	G191K2	. INTEGRATED CIRCUIT /49956/ /351-7101-022/	1	
- 5	F51K2	. INTEGRATED CIRCUIT /49956/ /351-7107-022/	2	
- 6	SF10112	. INTEGRATED CIRCUIT /93332/ /351-7297-022/	4	
- 7	SG8025	. INTEGRATED CIRCUIT /93332/ /351-7307-012/	1	
- 8	54L00SD7722A	. INTEGRATED CIRCUIT /12040/ /351-7365-012/	7	
- 9	54L10SD7723A	. INTEGRATED CIRCUIT /12040/ /351-7365-022/	2	
- 10	54L20SD7724A	. INTEGRATED CIRCUIT /12040/ /351-7365-032/	2	
- 11	54L72SD7730A	. INTEGRATED CIRCUIT /12040/ /351-7365-092.	1	
- 12	351-7436-012	. INTEGRATED CIRCUIT.	2	
- 13	G371K2	. INTEGRATED CIRCUIT /07933/ /351-7495-022/	3	
- 14	767-1421-001	. PEDESTAL, INTEGRATED CIRCUIT.	27	
- 15	352-0661-041	. TRANSISTOR.	3	
- 16	352-0551-041	. TRANSISTOR /EFF TO CI-70273/.	1	
- 16	352-7500-781	. TRANSISTOR /EFF WITH CI-70273/.	1	
- 17	353-2710-001	. DIODE /EFF TO CI-70273/	1	
- 17	353-2978-001	. DIODE /EFF CI-70273 TO CI-70423/.	1	
- 17	RCR05G682K	. RESISTOR /745-2371-000/ /EFF WITH CI-70423/	1	
- 18	353-2906-001	. DIODE /EFF TO CI-70273/	1	
- 18	353-3338-001	. DIODE /EFF WITH CI-70273/	1	
- 19	372-2621-045	. HOUSING, CONN	1	
- 19A	372-2621-015	. HOUSING, CONN	1	
- 20	372-2234-010	. CONTACT, ELEC	42	
- 21	RCR05G102JS	. RESISTOR /745-1863-490/	1	
- 22	RCR07G362JS	. RESISTOR /745-0768-000/ /EFF TO CI-70273/	1	
- 22	RCR05G332JS	. RESISTOR /745-1863-610/ /EFF WITH CI-70273/	1	
- 23	RCR07G392JS	. RESISTOR /745-0769-000/ /EFF TO CI-70273/	2	
- 23	RCR05G432JS	. RESISTOR /745-1863-640/ /EFF WITH CI-70273/	2	
- 24	RCR05G562JS	. RESISTOR /745-1863-670/	1	
- 25	RCR05G333JS	. RESISTOR /745-1863-850/	1	
- 26	RCR05G151K	. RESISTOR /745-2311-000/	1	
- 27	RCR05G102K	. RESISTOR /745-2341-000/	2	
- 28	RCR05G472K	. RESISTOR /745-2365-000/	3	
- 29	RCR05G822K	. RESISTOR /745-2374-000/	1	
- 30	RCR05G103K	. RESISTOR /745-2377-000/	1	
- 31	G5448X152M	. CAPACITOR, FXD, CER, 1500PF, 20%, 50V /96733/ /913-3244-270/. . /913-3244-270/	1	
- 32	G5448X182J	CAPACITOR, FXD, CER, DIEL, 1800PF, 5%, 50V /96733/. . . . . /913-3244-690/	1	
- 33	G5448X470J	. CAPACITOR, FXD, CER, 47PF, 5%, 50V /96733/ /913-3244-670/ . . . /EFF TO CI-70273/	1	
- 33	CK078X470K	. CAPACITOR /913-3287-040/ /EFF WITH CI-70273/.	1	
- 34	G5448X561J	. CAPACITOR, FXD, CER, 560PF, 5%, 50V /96733/ /913-3244-680/. . . /EFF TO CI-70273/	1	
- 34	CK078X561K	. CAPACITOR /913-3287-170/ /EFF WITH CI-70273/.	1	
- 35	CK318V513K	CAPACITOR /913-4500-230/.	1	
- 36	CK328V104M	CAPACITOR /913-4500-700/.	4	
- 37	M39003-01-2271	. CAPACITOR /184-9086-310/.	1	
- 38	600-9283-013	. BOARD	1	

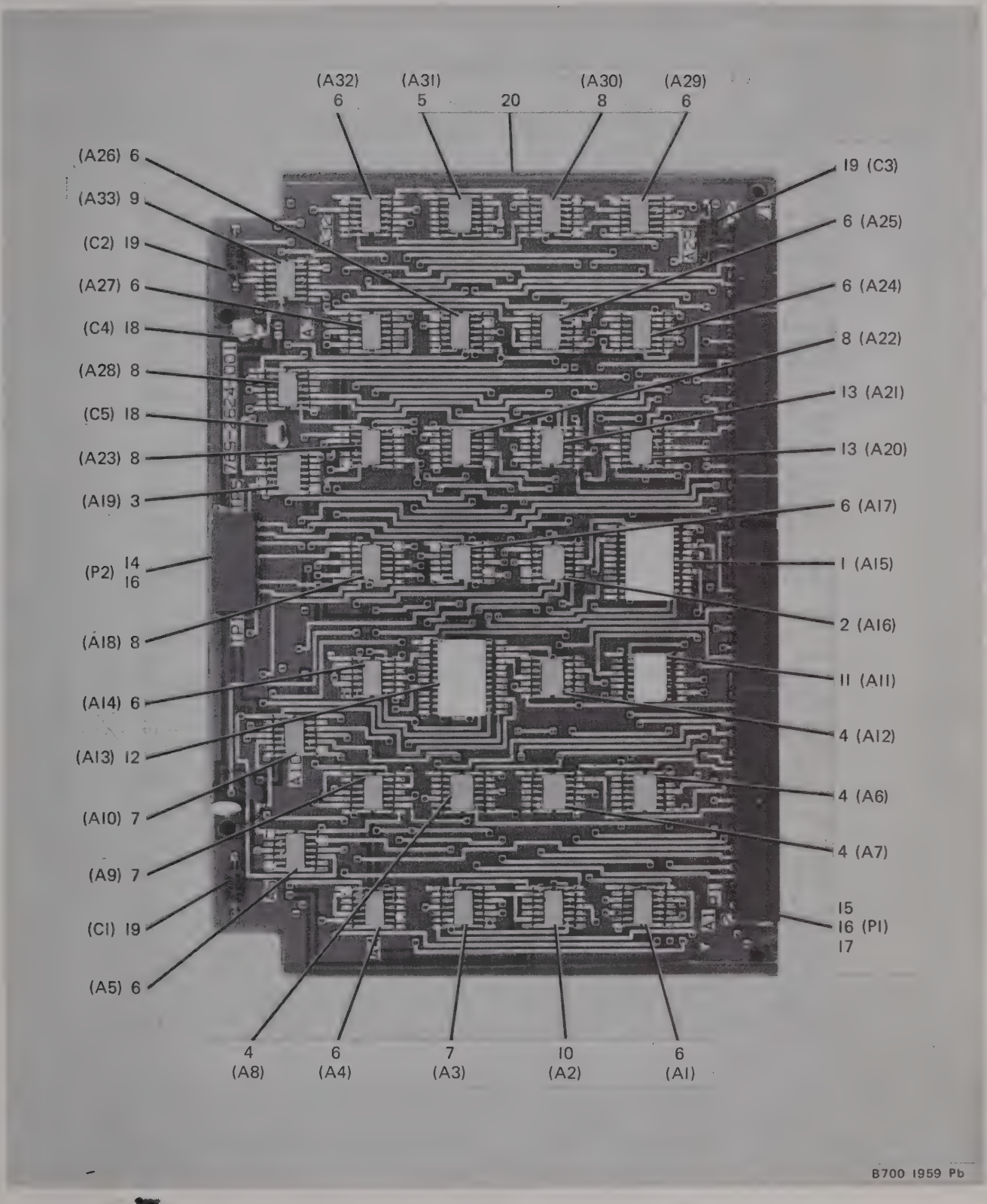


Figure 6-7. Instruction Decode Card A7A5

FIGURE AND INDEX NO.	PART NUMBER	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
7	789-2624-001 —	CARD, INSTRUCTION DECODE /SEE FIGURE 2 FOR NHA/	REF	
- 1	9261	. INTEGRATED CIRCUIT /07263/ /351-1025-012/	1	
- 2	SS14127	. INTEGRATED CIRCUIT /93332/ /351-7093-022/	1	
- 3	SS812	. INTEGRATED CIRCUIT /93332/ /351-7307-022/	1	
- 4	SS314	. INTEGRATED CIRCUIT /93332/ /351-7333-022/	4	
- 5	SM2014	. INTEGRATED CIRCUIT /93332/ /351-7341-012/	1	
- 6	54L00SD7722A	. INTEGRATED CIRCUIT /12040/ /351-7365-012/	11	
- 7	54L10SD7723A	. INTEGRATED CIRCUIT /12040/ /351-7365-022/	3	
- 8	SD7727A	. INTEGRATED CIRCUIT /12040/ /351-7365-062/	5	
- 9	54L72SD7730A	. INTEGRATED CIRCUIT /12040/ /351-7365-092/	1	
- 10	54L73SD8545A	. INTEGRATED CIRCUIT /12040/ /351-7365-102/	1	
- 11	HL11554	. INTEGRATED CIRCUIT /07263/ /351-7430-012/	1	
- 12	351-7437-012	. INTEGRATED CIRCUIT	1	
- 13	G371K2	. INTEGRATED CIRCUIT /07933/ /351-7495-022/	2	
- 14	372-2621-014	. HOUSING, CONN	1	
- 15	372-2623-045	. HOUSING, CONN	1	
- 16	372-2234-010	. CONTACT, ELEC	41	
- 17	372-2234-020	. CONTACT, ELEC	35	
- 18	G5448X181M	. CAPACITOR, FXD, CER, 180PF, 20%, 50V /96733/ /913-3244-160/ /EFF TO CI-70273/	2	
- 18	CK078X181K	. CAPACITOR /913-3287-110/ /EFF WITH CI-70273/	2	
- 19	CK323V104M	. CAPACITOR /913-4500-700/	3	
- 20	600-9286-010	. BOARD	1	

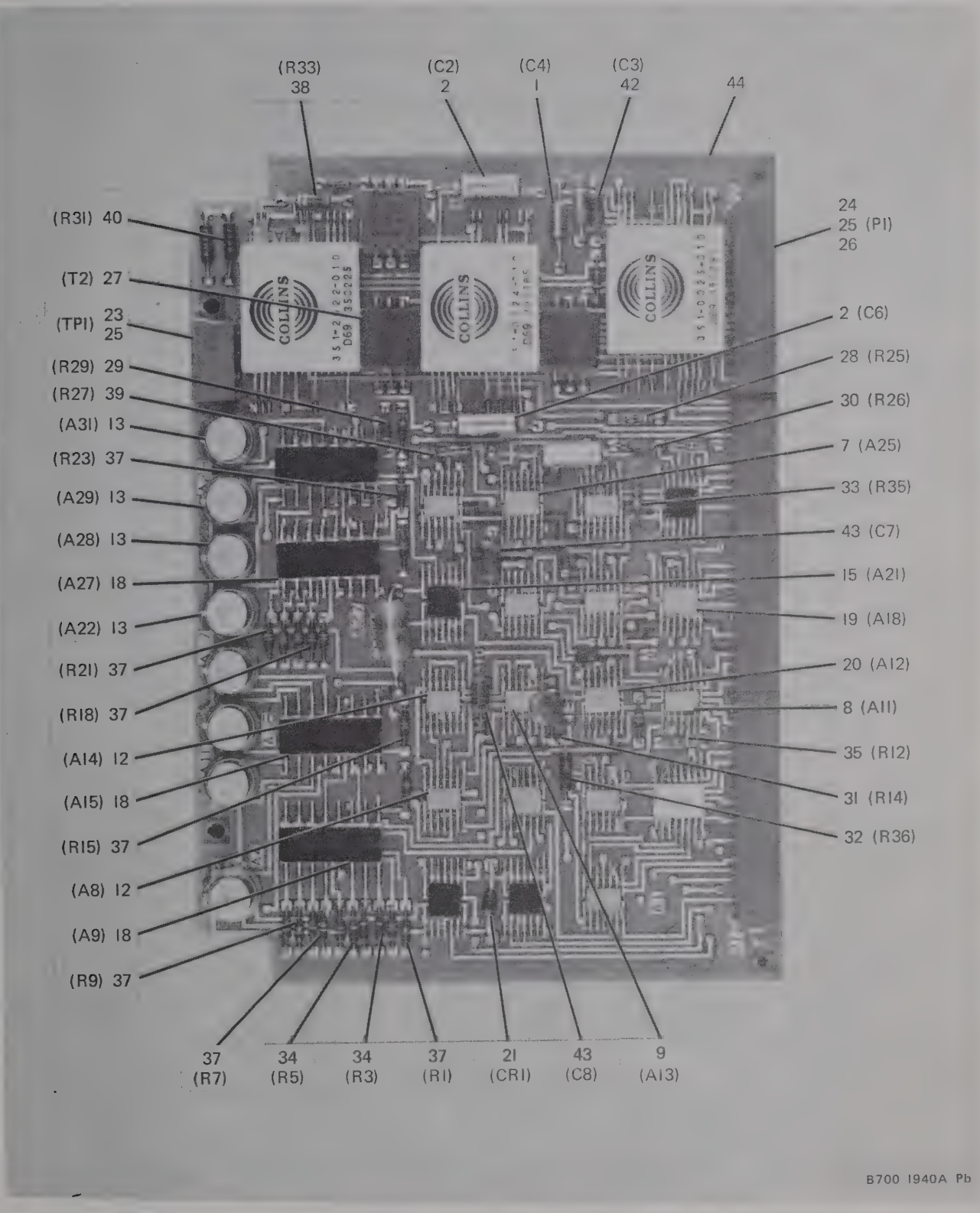


Figure 6-8. Accessible Memory Card A7A6 (Sheet 1 of 2)

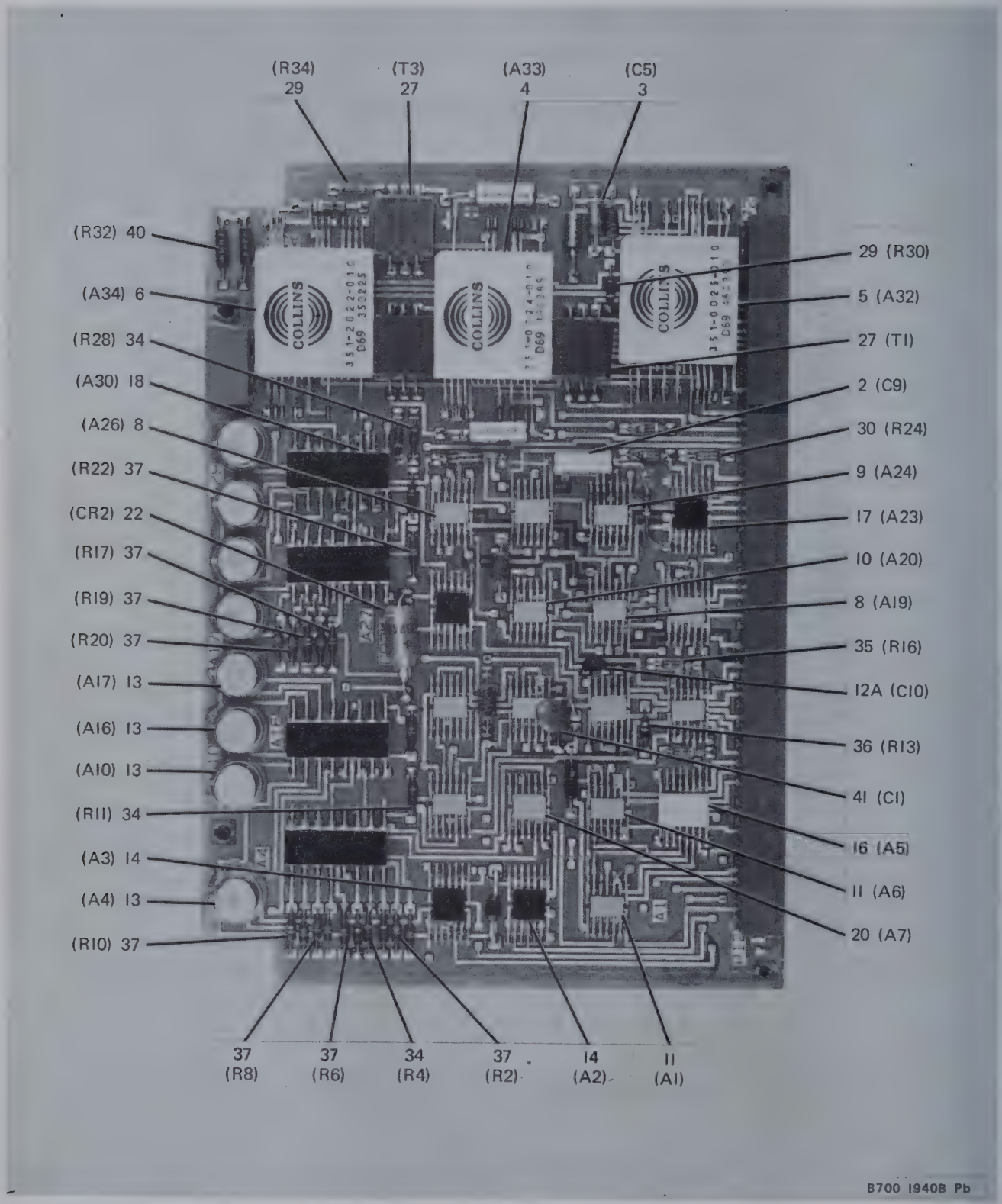


Figure 6-8. Accessible Memory Card A7A6 (Sheet 2 of 2)

FIGURE AND INDEX NO.	PART NUMBER	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
8	793-8982-001	CARD, ACCESSIBLE MEMORY /SEE FIGURE 2 FOR NHA/	REF	
- 1	M39003-01-2255	CAPACITOR /184-9086-150/	1	
- 2	M39003-01-2271	CAPACITOR /184-9086-310/	3	
- 3	M39003-01-2331	CAPACITOR /184-9087-180/	1	
- 4	351-0024-010	MICROCIRCUIT	1	
- 5	351-0025-010	MICROCIRCUIT	1	
- 6	351-2022-010	MICROCIRCUIT	1	
- 7	SG14127	INTEGRATED CIRCUIT /93332/ /351-7093-022/	1	
- 8	54L00SD7722A	INTEGRATED CIRCUIT /12040/ /351-7365-012/	3	
- 9	54L10SD7723A	INTEGRATED CIRCUIT /12040/ /351-7365-022/	2	
- 10	54L20SD7724A	INTEGRATED CIRCUIT /12040/ /351-7365-032/	1	
- 11	SD7726A	INTEGRATED CIRCUIT /12040/ /351-7365-052/	2	
- 12	54L73SN14834	INTEGRATED CIRCUIT /01295/ /351-7365-102/ /EFF TO CI-73033/	2	
- 12	54L73SD8545A	INTEGRATED CIRCUIT /12040/ /351-7365-102/ /EFF WITH CI-73033/	2	
- 12A	CK05BX222K	CAPACITOR /913-5019-120/ /EFF WITH CI-73033/ /USED WITH NATIONAL 54L73 IC ONLY/	1	
- 13	SM7037A	INTEGRATED CIRCUIT /27074/ /351-7398-032/	8	
- 14	HL11561	INTEGRATED CIRCUIT /07263/ /351-7428-012/	2	
- 15	12483	INTEGRATED CIRCUIT /07263/ /351-7429-012/	1	
- 16	351-7436-012	INTEGRATED CIRCUIT	1	
- 17	351-7445-012	INTEGRATED CIRCUIT	1	
- 18	A7K3705L422A	INTEGRATED CIRCUIT /07263/ /351-7449-012/ /EFF TO REV LTR BC/	4	
- 18	3705DMQB	INTEGRATED CIRCUIT /07263/ /351-7449-021/ /EFF WITH REV LTR BC/	4	
- 19	G380K2	INTEGRATED CIRCUIT /49956/ /351-7452-012/	1	
- 20	G371K2	INTEGRATED CIRCUIT /07933/ /351-7495-022/	2	
- 21	353-6522-041	DIODE /EFF TO CI-71423/	1	
- 21	353-9010-261	DIODE /EFF WITH CI-71423/	1	
- 22	353-3129-001	DIODE /EFF TO CI-71283/	1	
- 22	353-901C-201	DIODE /EFF WITH CI-71283/	1	
- 23	372-2621-013	HOUSING, CONN	1	
- 24	372-2623-045	HOUSING, CONN	1	
- 25	372-2234-010	CONTACT, ELEC	36	
- 26	372-2234-020	CONTACT, ELEC	33	
- 27	317-187	TRANSFORMER, AF /06973/ /677-9524-010/	3	
- 28	RCR05G910JS	RESISTOR /745-1863-240/	1	
- 29	RCR05G431JS	RESISTOR /745-1863-410/	3	
- 30	RCR05G561JS	RESISTOR /745-1863-430/	2	
- 31	RCR05G103K	RESISTOR /745-2377-000/ /EFF TO CI-71203/	1	
- 31	RCR05G682JS	RESISTOR /745-1863-690/ /EFF WITH CI-71203/	1	
- 32	RCR05G103JS	RESISTOR /745-1863-730/ /EFF WITH CI-71203/	1	
- 33	RCR05G680K	RESISTOR /745-2298-000/	1	
- 34	RCR05G272K	RESISTOR /745-2356-000/	5	
- 35	RCR05G472K	RESISTOR /745-2365-000/	2	
- 36	RCR05G103K	RESISTOR /745-2377-000/	1	
- 37	RCR05G223K	RESISTOR /745-2389-000/	15	
- 38	RCR05G681JS	RESISTOR /745-1863-450/	AR	
- 38	RCR05G102JS	RESISTOR /745-1863-490/	AR	
- 38	RCR05G152JS	RESISTOR /745-1863-530/	AR	
- 38	RCR05G222JS	RESISTOR /745-1863-570/	AR	
- 38	RCR05G332JS	RESISTOR /745-1863-610/	AR	
- 38	RCR05G392JS	RESISTOR /745-1863-630/	AR	
- 38	RCR05G472JS	RESISTOR /745-1863-650/	AR	
- 38	RCR05G562JS	RESISTOR /745-1863-670/	AR	
- 38	RCR05G682JS	RESISTOR /745-1863-690/	AR	
- 38	RCR05G822JS	RESISTOR /745-1863-710/	AR	
- 38	RCR05G103JS	RESISTOR /745-1863-730/	AR	
- 38	RCR05G123JS	RESISTOR /745-1863-750/	AR	
- 38	RCR05G153JS	RESISTOR /745-1863-770/	AR	
- 38	RCR05G183JS	RESISTOR /745-1863-790/	AR	
- 38	RCR05G223JS	RESISTOR /745-1863-810/	AR	
- 38	RCR05G273JS	RESISTOR /745-1863-830/	AR	
- 38	RCR05G333JS	RESISTOR /745-1863-850/	AR	
- 39	RNR55J2742FM	RESISTOR /705-1499-430/	AR	
- 39	RNR55J2802FM	RESISTOR /705-1499-440/	AR	
- 39	RNR55J2872FM	RESISTOR /705-1499-450/	AR	
- 39	RNR55J2942FM	RESISTOR /705-1499-460/	AR	
- 39	RNR55J3012FM	RESISTOR /705-1499-470/	AR	
- 39	RNR55J3092FM	RESISTOR /705-1499-480/	AR	
- 39	RNR55J3162FM	RESISTOR /705-1499-490/	AR	
- 39	RNR55J3242FM	RESISTOR /705-1499-500/	AR	
- 39	RNR55J3322FM	RESISTOR /705-1499-510/	AR	
- 40	RNR55J6492FM	RESISTOR /705-1499-790/	AR	
- 40	RNR55J6652FM	RESISTOR /705-1499-800/	AR	
- 40	RNR55J6812FM	RESISTOR /705-1499-810/	AR	
- 40	RNR55J6982FM	RESISTOR /705-1499-820/	AR	
- 40	RNR55J7152FM	RESISTOR /705-1499-830/	AR	
- 40	RNR55J7322FM	RESISTOR /705-1499-840/	AR	
- 40	RNR55J7502FM	RESISTOR /705-1499-850/	AR	
- 40	RNR55J7682FM	RESISTOR /705-1499-860/	AR	
- 40	RNR55J7872FM	RESISTOR /705-1499-870/	AR	
- 41	G544BX152M	CAPACITOR, FXD, CER, 1500PF, 20%, 50V /96733/ /913-3244-270/ /EFF TO CI-71253/	1	
- 41	[illegible]8X561K	CAPACITOR /913-3287-170/ /EFF WITH CI-71253/	1	
- 42	CK31BT392K	CAPACITOR /913-4500-080/	1	
- 43	CK32BV104M	CAPACITOR /913-4500-700/	2	
- 44	600-9364-010	BOARD	1	

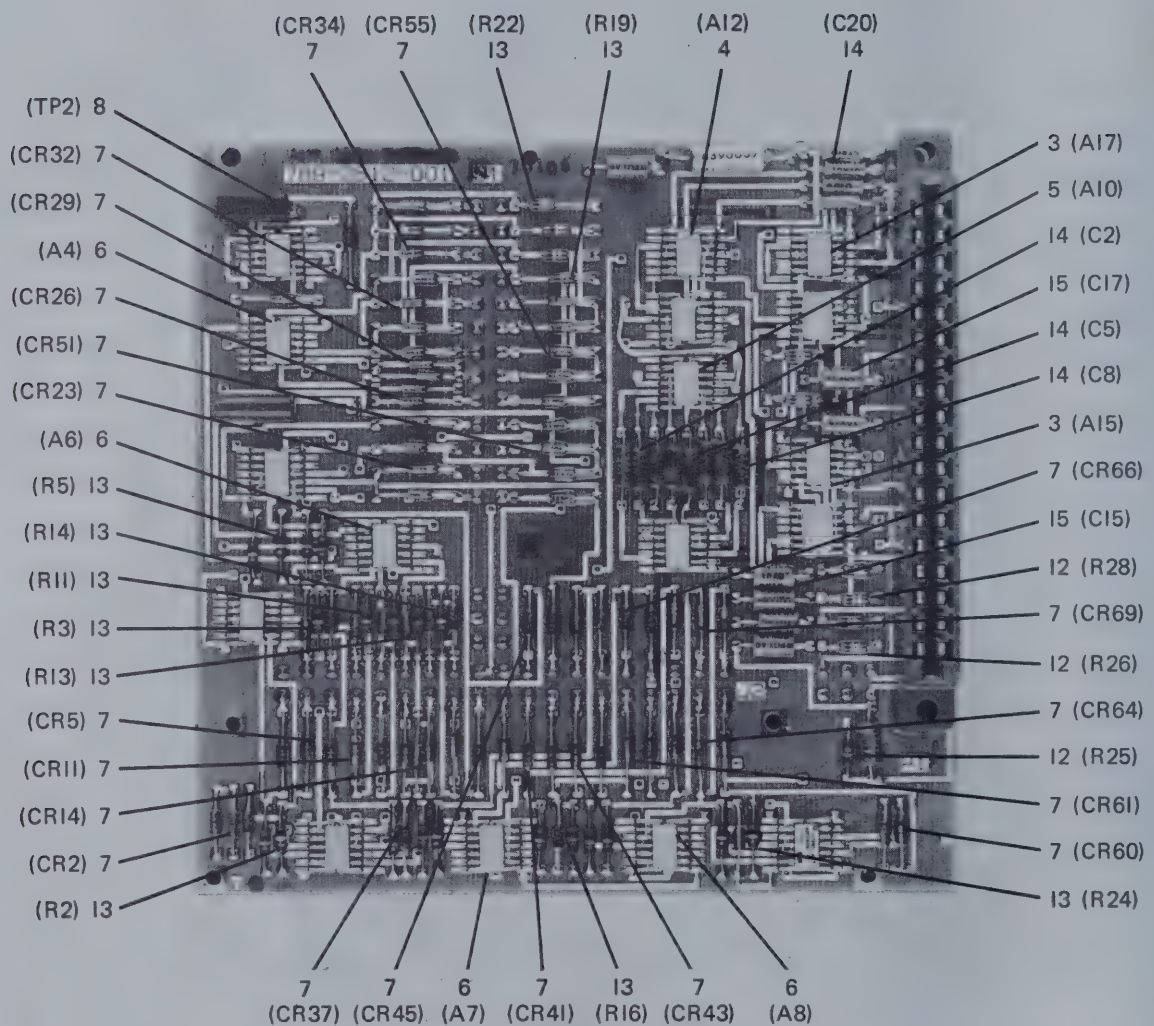


Figure 6-9. Matrix Card A7A7 (Sheet 1 of 3)

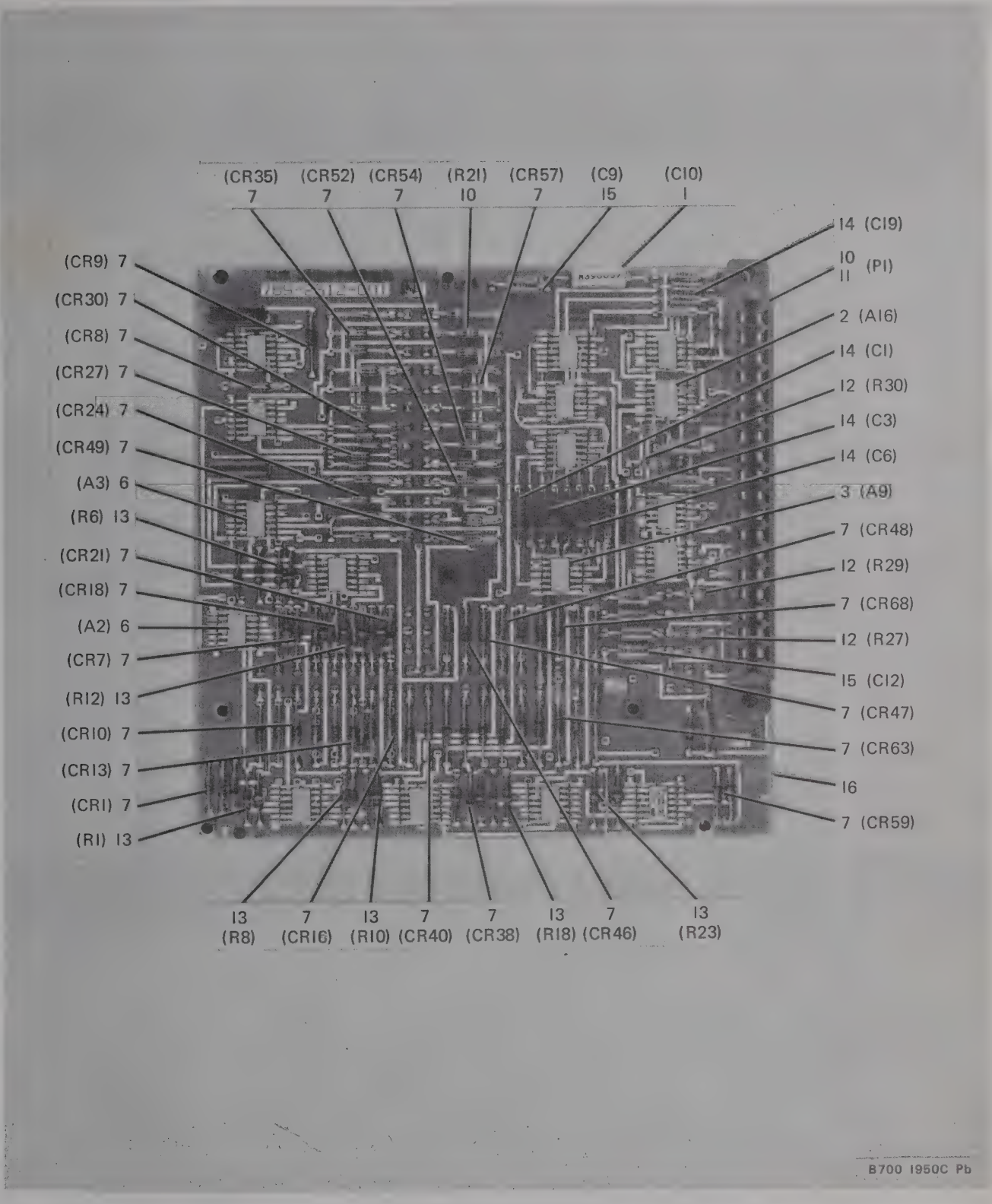


Figure 6-9. Matrix Card A7A7, A8A2 (Sheet 2 of 3)

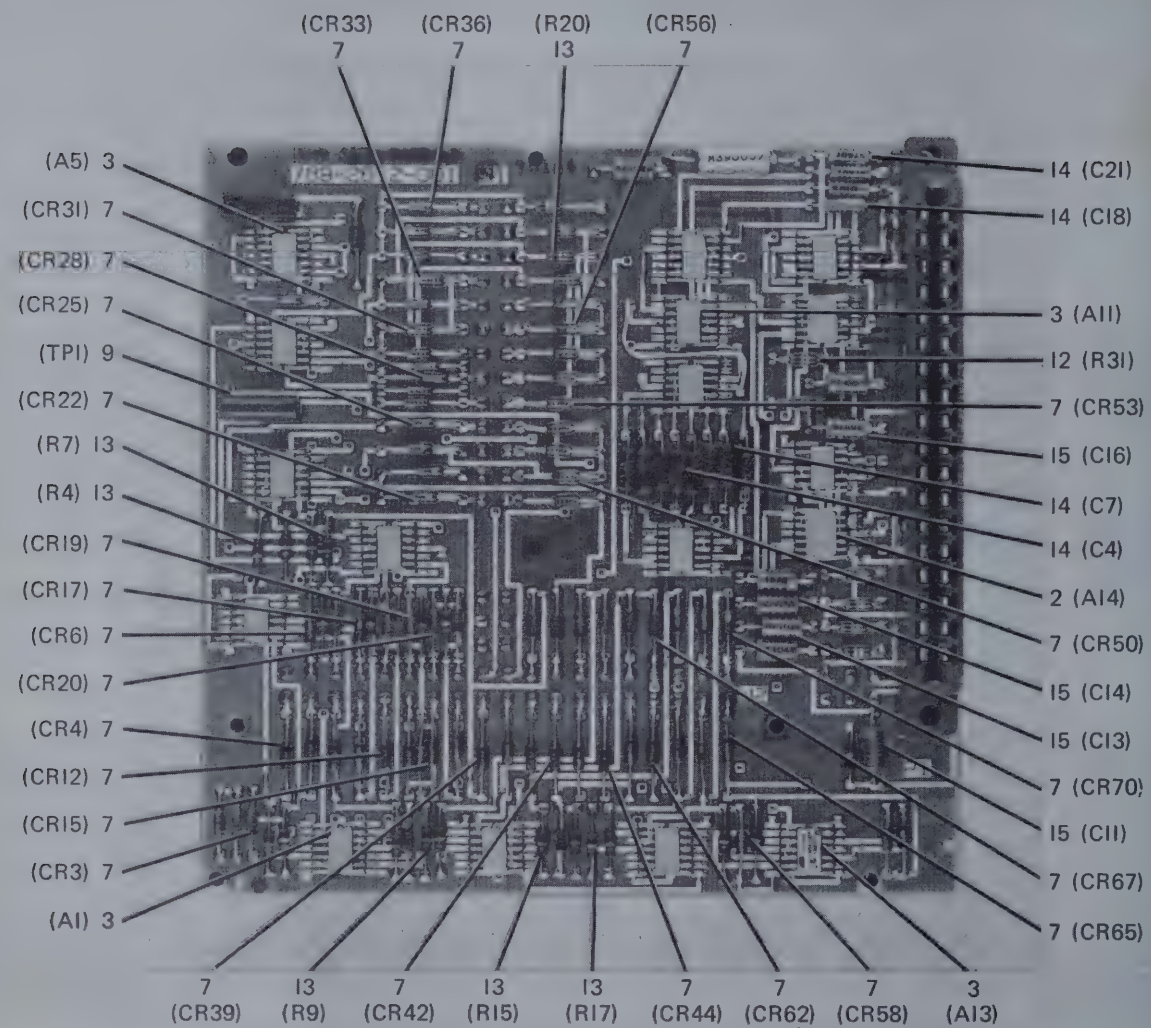


Figure 6-9. Matrix Card A7A7, A8A2 (Sheet 3 of 3)

FIGURE AND INDEX NO.	PART NUMBER	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
9	789-2612-001	CARD, MATRIX /SEE FIGURES 2 AND 13 FOR NHA/	REF	
- 1	M39003-01-2272	. CAPACITOR /184-9086-320/	1	
- 2	SG14127	. INTEGRATED CIRCUIT /93332/ /351-7093-022/	2	
- 3	54L00SD7722A	. INTEGRATED CIRCUIT /12040/ /351-7365-012/	7	
- 4	54L20SD7724A	. INTEGRATED CIRCUIT /12040/ /351-7365-032/	1	
- 5	54L30SD7725A	. INTEGRATED CIRCUIT /12040/ /351-7365-042/	1	
- 6	SD9857A	. INTEGRATED CIRCUIT /27014/ /351-7390-012/	6	
- 7	353-3656-031	. DIODE	70	
- 8	M39024-11-03	. JACK /360-0161-000/	1	
- 9	M39024-11-04	. JACK /360-0162-000/	1	
- 10	372-2601-057	. CONTACT, ELEC	76	
- 11	M21097-1-136	. CONNECTOR /372-7502-340/	1	
- 12	RCR05G103JS	. RESISTOR /745-1863-730/	7	
- 13	RCR05G104JS	. RESISTOR /745-1864-010/	24	
- 14	CK31BT102M	. CAPACITOR, FXD, GL, 1000PF, 20%, 50V /16299/ /913-4500-360/ /EFF TO CI-71354/	12	
- 14	CK31BT102K	. CAPACITOR /913-4500-010/ /EFF WITH CI-71354/	12	
- 15	CK32BV104M	. CAPACITOR /913-4500-700/	8	
- 16	600-9283-011	. BOARD	1	

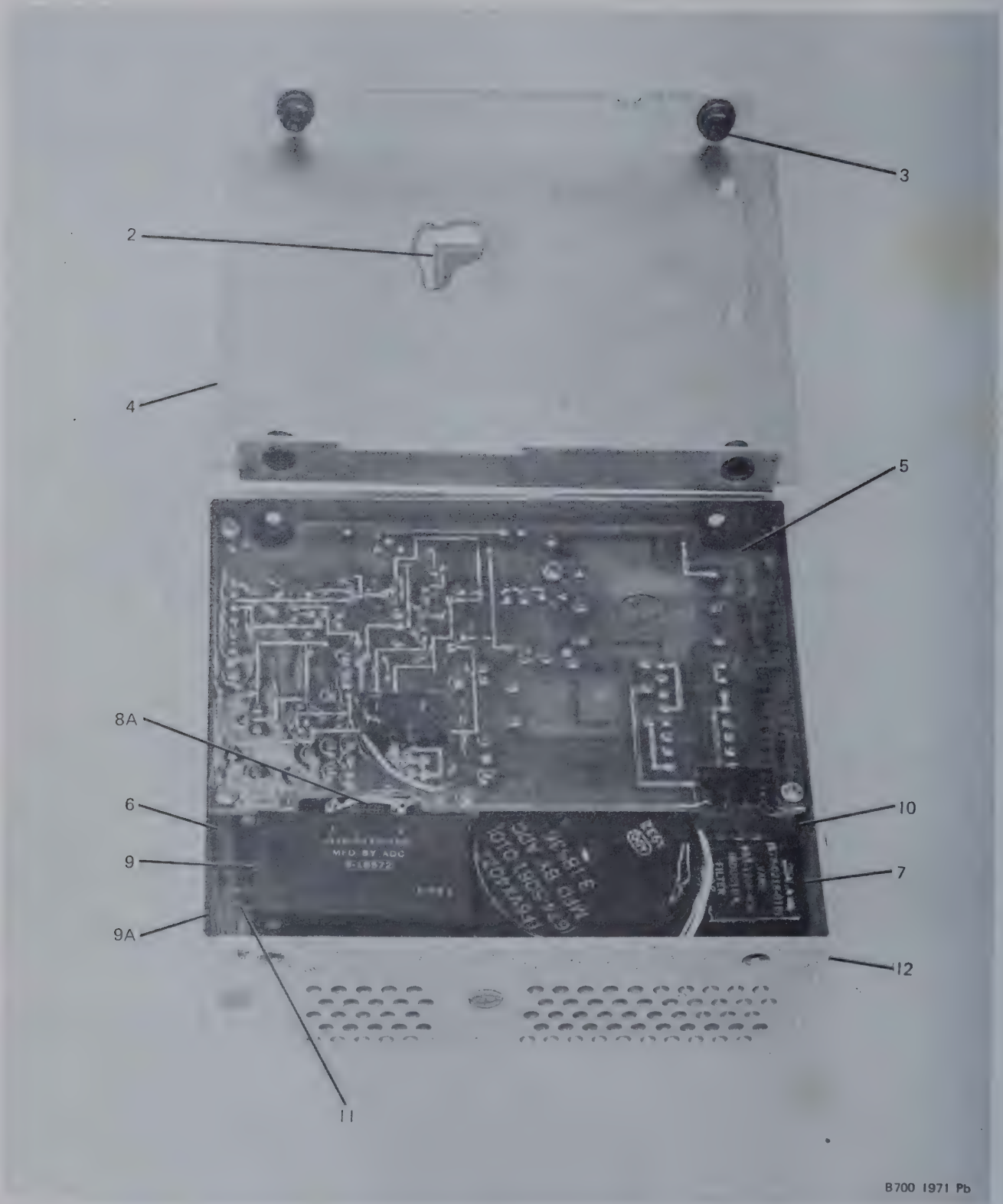


Figure 6-10. Power Supply A7A10PS1, A8A5PS1 (Sheet 1 of 2)

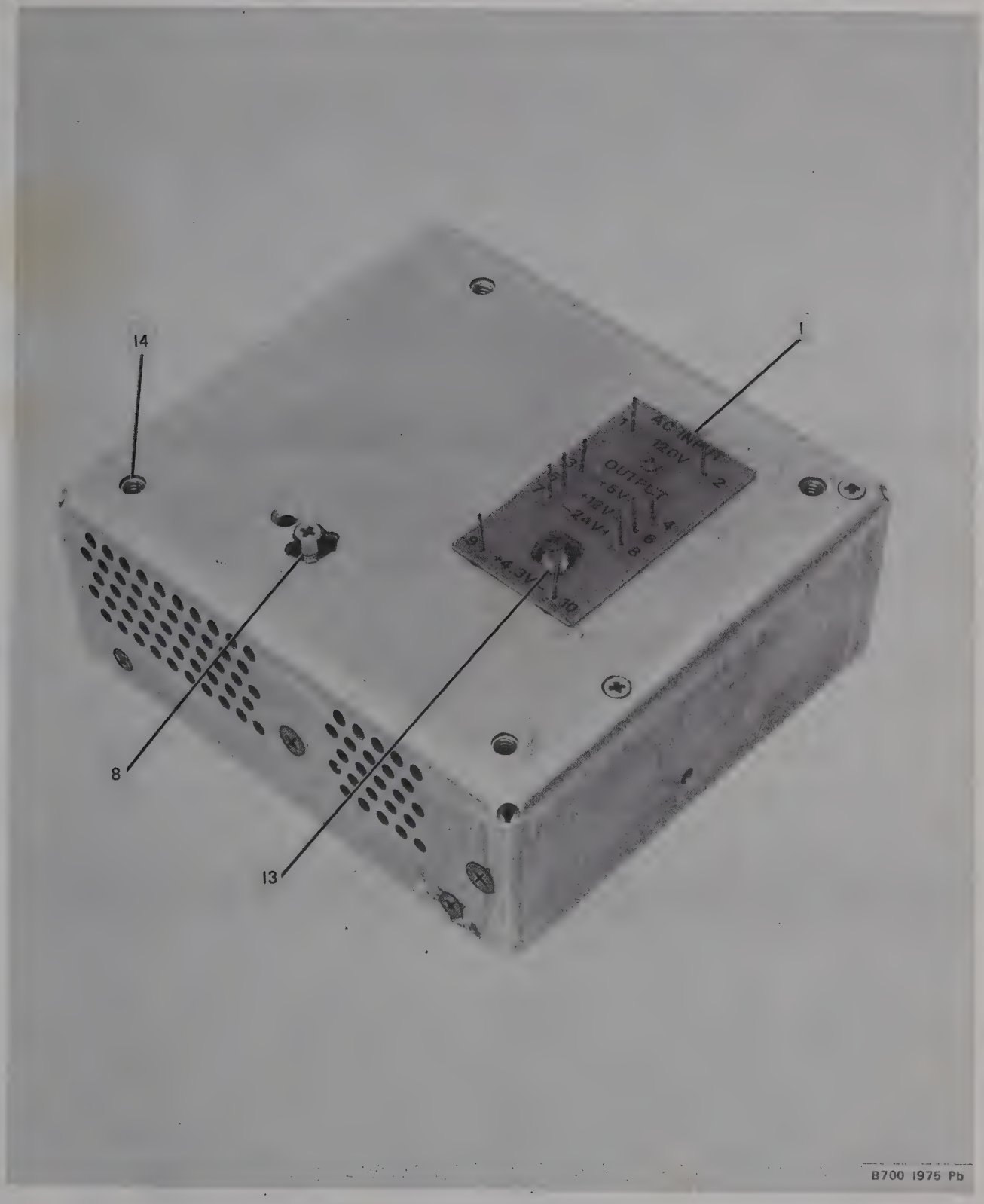


Figure 6-10. Power Supply A7A10PS1, A8A5PS1 (Sheet 2 of 2)

FIGURE AND INDEX NO.	PART NUMBER	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
10	793-9305-001	POWER SUPPLY /SEE FIGURE 2 AND 13 FOR NHA/.	REF	
- 1	610-1524-001	. INSULATOR	1	
		-ATTACHING PARTS		
	MS51957-13	. SCREW /343-0133-000/.	2	
	MS27183-3	. WASHER /310-0731-030/	2	
	310-0277-000	. WASHER, LOCK, SST, 0.102 ID X 0.198 OD /70318/ /310-0277-000/	2	
		---•---		
	793-3378-001	. COVER, POWER SUPPLY	1	
		-ATTACHING PARTS		
	MS51959-14	. SCREW /342-0045-000/.	4	
		---•---		
- 2	280-1339-130	. . LABEL, HIGH VOLTAGE /16319/ /280-3037-000/.	1	
- 3	FPN4-40SCL	. . NUT, PRESS, CD PL STL, 4-40 /83324/ /334-1151-000/.	4	
- 4	793-3378-002	. . COVER, POWER SUPPLY	1	
- 5	793-9321-001	. BOARD, CONTROL /SEE FIGURE 11 FOR BREAKDOWN/.	1	
		-ATTACHING PARTS-		
	MS51957-13	. SCREW /343-0133-000/.	4	
	MS27183-3	. WASHER /310-0731-030/	4	
	310-0277-000	. WASHER, LOCK, SST, 0.102 ID X 0.198 OD /70318/ /310-0277-000/	4	
		---•---		
- 6	540-9054-003	. POST.	2	
- 7	793-9322-001	. BOARD, INVERTER /SEE FIGURE 12 FOR BREAKDOWN/	1	
		-ATTACHING PARTS		
	MS51959-12	. SCREW /342-0043-000/.	3	
	MS51957-13	. SCREW /343-0133-000/.	1	
	MS27183-3	. WASHER /310-0731-030/	1	
	310-0277-000	. WASHER, LOCK, SST, 0.102 ID X 0.198 OD /70318/ /310-0277-000/	1	
		---•---		
- 8	541-5979-002	. SLEEVE.	1	
		-ATTACHING PARTS		
	MS51959-17	. SCREW /342-0048-000/.	1	
		---•---		
- 8A	1N647	. DIODE /353-2852-000/ /EFF TO CI-71337/.	1	
- 8A	353-2852-001	. DIODE /EFF WITH CI-71337/	1	
- 9	3-18572	. INDUCTOR /70674/ /678-0235-010/	1	
		-ATTACHING PARTS-		
	MS51959-27	. SCREW /342-0061-000/.	2	
	68NM62	. NUT, SLFLKG, HEX, AL, 6-32 /72962/ /333-0368-000/	2	
		---•---		
- 9A	RH5X000B10001F	. RESISTOR, FXD, WW, 10K OHMS, 1%, 5W /91637/ /747-0984-470/.	1	
		-ATTACHING PARTS-		
	MS51959-4	. SCREW /342-0134-000/.	2	
	310-0070-000	. WASHER, LOCK, SST, 0.151 ID X 0.165 OD /79807/ /310-0070-000/	2	
	MS35649-224	. NUT /313-0037-000/.	2	
		---•---		
- 10	540-9054-003	. POST.	2	
		-ATTACHING PARTS		
	MS51957-13	. SCREW /343-0133-000/.	2	
	MS27183-3	. WASHER /310-0731-030/	2	
	310-0277-000	. WASHER, LOCK, SST, 0.102 ID X 0.198 OD /70318/ /310-0277-000/	2	
	302-4800-000	. WASHER, NM, FBR, 0.116 ID X 1/4 OD /74921/ /302-4800-000/	2	
		---•---		
- 11	540-9033-003	. POST.	2	
		-ATTACHING PARTS-		
	MS51959-17	. SCREW /342-0048-000/.	2	
		---•---		
- 12	610-1501-001	. CHASSIS, POWER SUPPLY	1	
		PARTIAL BREAKDOWN FOLLOWS		
- 13	NCN4-1-3	. . NUT, CAPTIVE, SST, 4-40 /07886/ /334-0442-000/.	2	
- 14	CL832-2C	. . NUT, PLAIN, CL, CD PL STL, 8-32 /46384/ /334-0559-000/.	4	

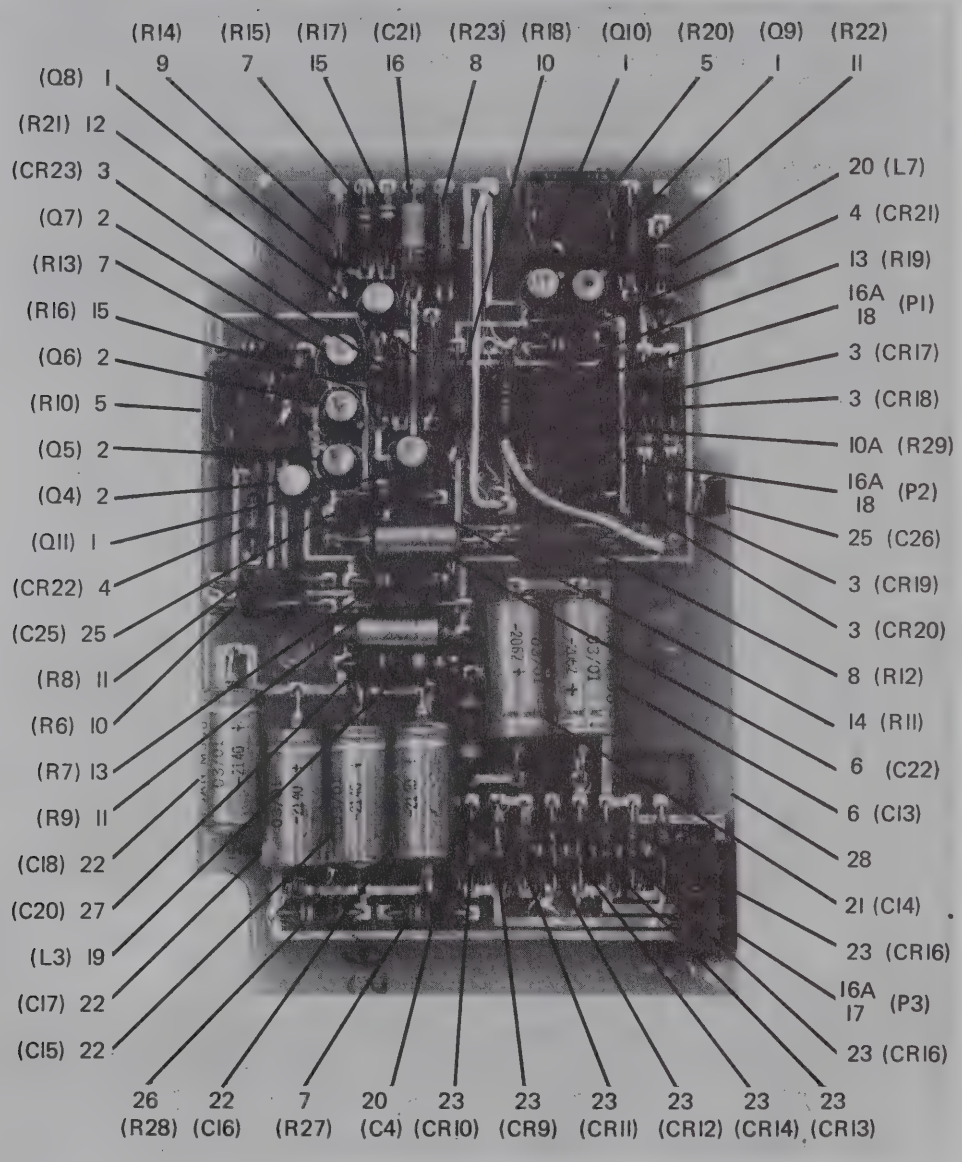


Figure 6-11. Control Board A7A10PS1A1, A8A5PS1A1

FIGURE AND INDEX NO.	PART NUMBER	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
11	793-9321-001	BOARD, CONTROL /SEE FIGURE 10 FOR NHA/	REF	
- 1	352-7500-281	. TRANSISTOR	4	
- 2	352-7500-191	. TRANSISTOR	4	
- 3	353-9008-011	. DIODE	5	
- 4	353-3625-011	. DIODE	2	
- 5	RT22C2P101	. RESISTOR /381-1721-010/	2	
- 6	M39003-01-2005	. CAPACITOR /184-9083-050/	1	
- 7	RCR07G103KS	. RESISTOR /745-0785-000/	3	
- 8	RNC6CH1000FR	. RESISTOR /724-1015-150/	2	
- 9	RNC6CH1101FR	. RESISTOR /724-1015-650/	1	
- 10	RNC60H7500FR	. RESISTOR /724-1015-570/	2	
- 10A	RN6CD1961F	. RESISTOR /705-6610-000/ /EFF WITH CI-72263/	1	
- 11	RNC6CH5110FR	. RESISTOR /724-1015-490/	3	
- 12	RNC6CH5620FR	. RESISTOR /724-1015-510/	1	
- 13	RCR07G221KS	. RESISTOR /745-0725-000/	2	
- 14	RCR07G820KS	. RESISTOR /745-0710-000/	1	
- 15	RCR07G220KS	. RESISTOR /745-0689-000/	2	
- 16	C22A223K	. CAPACITOR, FXD, CER, 22,000PF, 10%, 100/ /16546/ /913-5661-160/	1	
- 16A	372-2252-010	. CONTACT, ELEC	15	
- 17	372-2624-011	. HOUSING, CONN, DBL ROW	1	
- 18	372-2625-017	. HOUSING, CONN, SGL ROW	1	
- 19	MS90537-41	. INDUCTOR /240-2715-410/	1	
- 20	MS90537-30	. INDUCTOR /240-2715-300/	2	
- 21	M39003-01-2062	. CAPACITOR /184-9083-620/	2	
- 22	M39003-01-2140	. CAPACITOR /184-9084-670/	4	
- 23	353-3337-001	. DIODE	8	
- 23	JAN1N4500	. DIODE /353-9008-190/	8	
- 24	7717-16DAP	. INSULATOR, DISK /13103/ /352-9552-230/	8	
- 25	CK05BX470K	. CAPACITOR /913-4002-000/	2	
- 26	RCR07G682KS	. RESISTOR /745-0779-000/	1	
- 27	M39003-01-2047	. CAPACITOR /184-9083-470/	1	
- 28	600-0133-011	. BOARD	1	

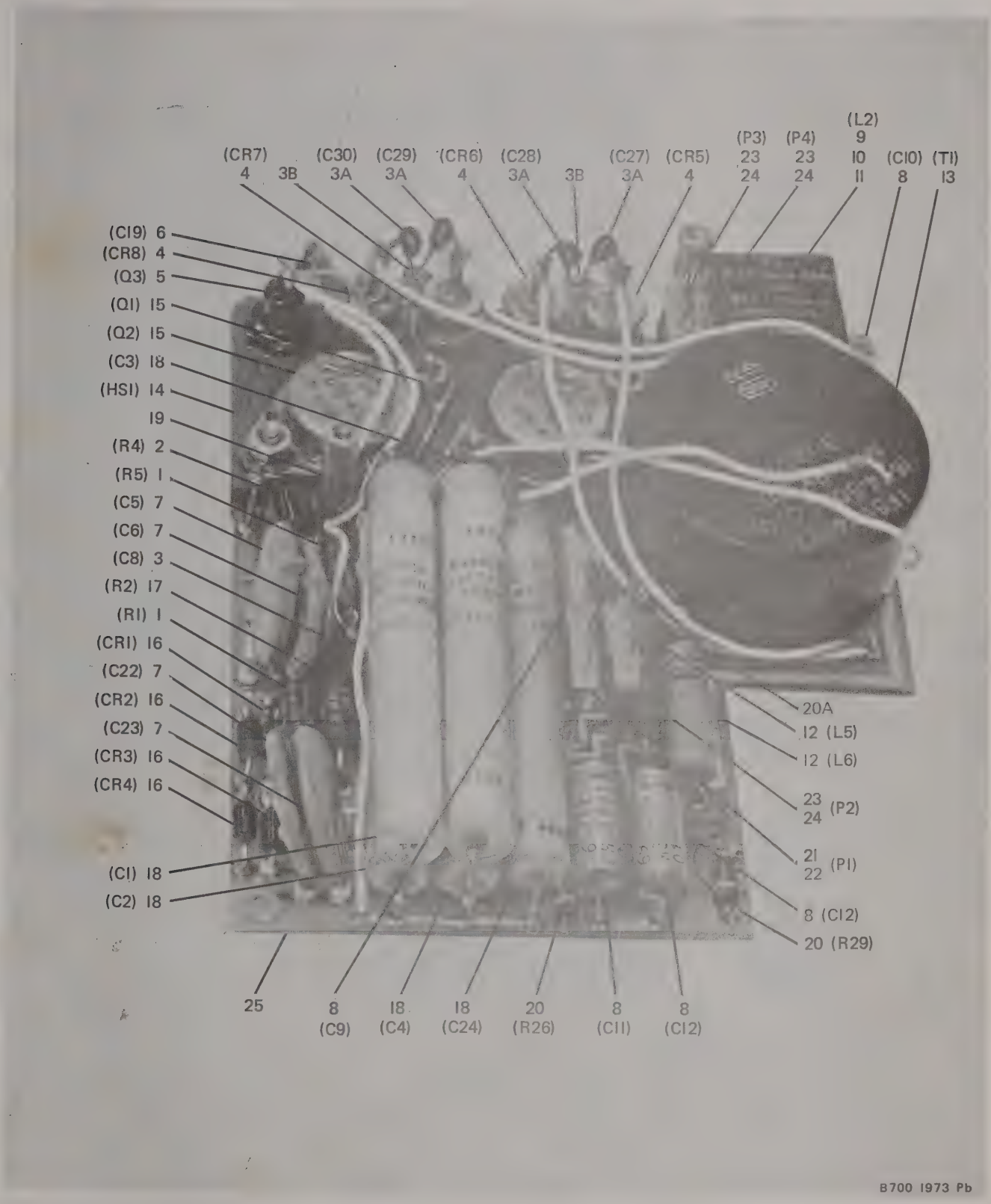


Figure 6-12. Inverter Board A7A10PS1A2, A8A5PS1A2

FIGURE AND INDEX NO.	PART NUMBER	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
12	793-9322-001	BOARD, INVERTER /SEE FIGURE 10 FOR NHA/	REF	
- 1	RW69V2R7	. RESISTOR /747-5364-000/	2	
- 2	RW69V151	. RESISTOR /747-5385-000/	1	
- 3	CK63CZ332M	. CAPACITOR /913-4495-510/.	1	
- 3A	CM05FD391GP3	. CAPACITOR /912-4156-920/ /EFF WITH CI-72283/.	4	
- 3B	2115	. TERMINAL, LUG /304-1466-010/ /EFF WITH CI-72283/.	2	
- 4	353-9009-011	. DIODE	4	
		-ATTACHING PARTS-		
	334-1008-000	. NUT, HEX, BRS, DBL CHAM, 10-32.	4	
	310-0081-000	. WASHER, LOCK, BRZ, 0.194 ID X 0.323 OD /79807/ /310-0081-000/	4	
		---*---		
- 5	353-6080-001	. TRANSISTOR.	1	
		-ATTACHING PARTS-		
	334-1008-000	. NUT, HEX, BRS, DBL CHAM, 10-32.	1	
	310-0081-000	. WASHER, LOCK, BRZ, 0.194 ID X 0.323 OD /79807/ /310-0081-000/	1	
		---*---		
- 6	CK63AW103M	. CAPACITOR /913-1188-000/.	1	
- 7	41C92	. CAPACITOR, FXD, CER, 0.1UF, M20%, P80%, 500V /01939/. /913-3152-000/	4	
- 8	M39003-01-2026	. CAPACITOR /184-9083-260/.	4	
- 9	953-1208-400	. INDUCTOR, FILTER, 12 UH /83003/ /678-0218-010/.	1	
		-ATTACHING PARTS-		
- 10	MS51957-3	. SCREW /343-0124-000/.	1	
	310-6320-000	. WASHER, FLAT, SST, 0.092 ID X 0.218 OD /79807/ /310-6320-000/	1	
	302-7000-000	. WASHER, FIBER, 0.156 ID X 0.375 OD /77921/ /302-7000-000/ /EFF TO CI-72263/	1	
	5602-10-62	. WASHER, NON-METALLIC, 0.125 ID X 0.312 OD /86928/ /302-0642-160/ /EFF WITH CI-72263/ DELETE /EFF WITH REV LTR AE/	1	
- 11	MS51957-3	. SCREW /343-0124-000/.	1	
	310-6320-000	. WASHER, FLAT, SST, 0.092 ID X 0.218 OD /79807/ /310-6320-000/	1	
	5602-58-16	. WASHER, FBR, NM, 0.115 ID X 0.199 OD /86928/ /302-0642-130/	1	
		---*---		
- 12	MS91189-30	. INDUCTOR /240-2691-170/	2	
- 13	3-18536	. TRANSFORMER /70674/ /674-5081-010/.	1	
- 14	793-3374-001	. BAR	1	
- 15	352-7500-491	. TRANSISTOR.	2	
		-ATTACHING PARTS-		
	P343-0333-000	. SCREW, MACH, NP BRS, 6-32 X 5/8 /77250/ /343-0333-000/ /EFF TO CI-72263/	4	
	P343-0290-000	. SCREW, MACH, NP, BRS, 4-40 X 5/8 IN. LG /77250/ /343-0290-000/. /EFF WITH CI-72263/	4	
	310-0055-000	. WASHER, FLAT, BRS, 0.147 ID X 0.312 OD /79607/ /310-0055-000/ /EFF TO CI-72263/	8	
	310-0054-000	. WASHER, FLAT, BRS, 0.125 ID X 0.312 OD /79807/ /310-0054-000/ /EFF WITH CI-72263/	8	
	310-0131-000	. WASHER, FLAT, BRS, 0.125 ID X 1/4 OD /EFF WITH REV LTR AE/.	8	
	MS35338-136	. WASHER /310-0282-000/ /EFF TO CI-72263/	4	
	MS35338-135	. WASHER /310-0279-000/ /EFF WITH CI-72263/	4	
	P313-0140-000	. NUT, PLAIN, HEX, NP BRS, 6-32 /77250//313-0140-000/ /EFF TO CI-72263/	4	
	P313-0156-000	. NUT, PLAIN, HEX, NP, BRS, 4-40 /77250/ /313-0156-000/ /EFF WITH CI-72263/	4	
		---*---		
- 16	353-9009-061	. DIODE	4	
- 17	RW69V1R8	. RESISTOR /747-5305-000/	1	
- 18	M39018-01-0674	. CAPACITOR /184-5103-690/.	5	
- 19	607-7710-001	. SPACER.	1	
- 20	RCR07G102KS	. RESISTOR /745-0749-000/	2	
- 20A	372-2236-010	. CONTACT, ELECTRICAL	14	
	607-7703-001	. PIN ASSEMBLY.	1	
- 21	372-2602-012	. . CONTACT, ELEC /EFF TO REV LTR AD/	3	
- 21	372-2602-013	. . CONTACT, ELEC /EFF WITH REV LTR AD/	3	
- 22	372-2235-010	. . HOUSING, CONTACT.	1	
	607-7702-001	. PIN ASSEMBLY.	3	
- 23	372-2602-012	. . CONTACT, ELEC /EFF TO REV LTR AD/	4	
- 23	372-2602-013	. . CONTACT, ELEC /EFF WITH REV LTR AD/	3	
- 24	372-2235-010	. . HOUSING, CONTACT.	1	
- 25	600-0133-012	. BOARD	1	

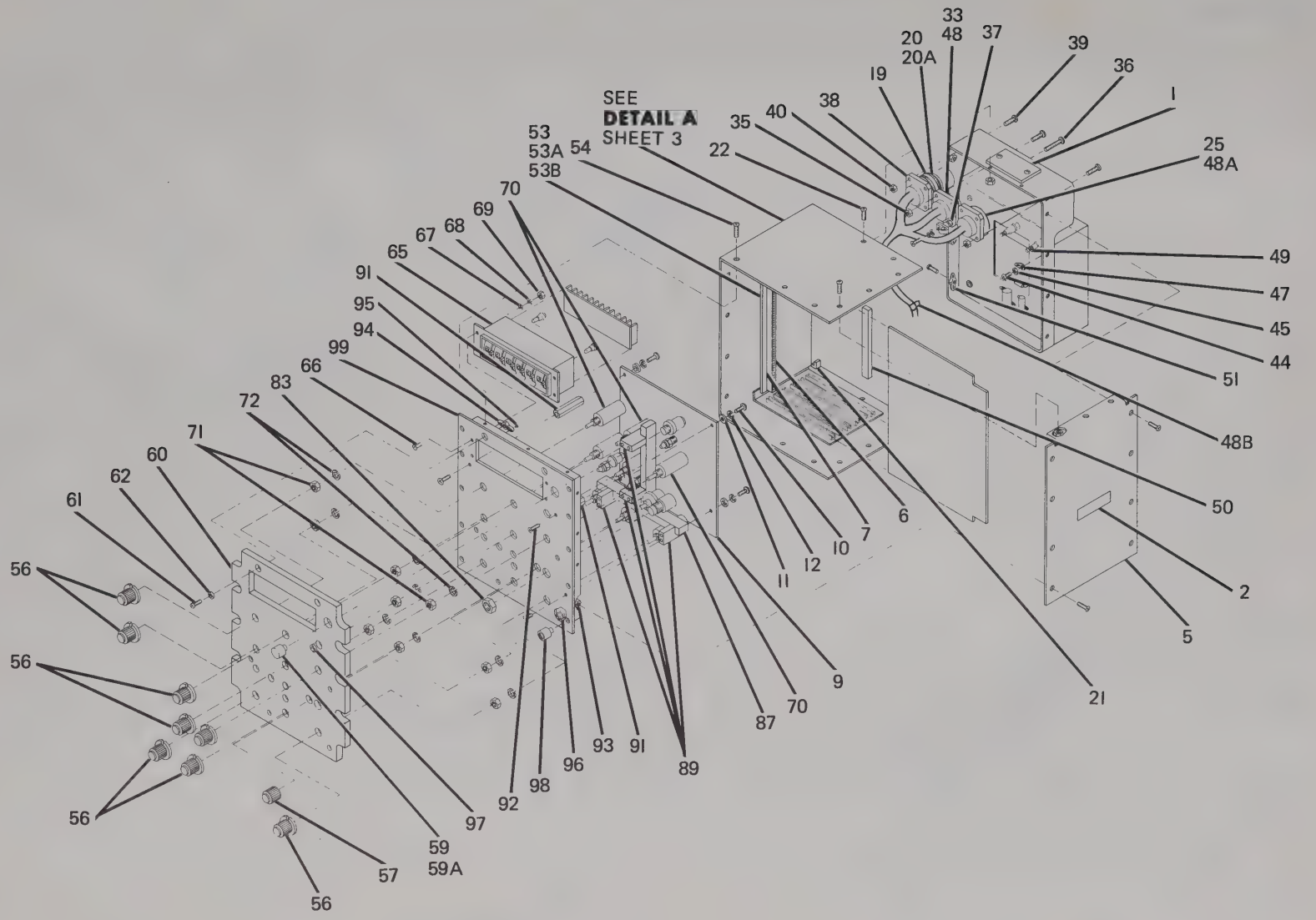


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Figure 6-13. Receive Control Head A8 (Sheet 1 of 3)

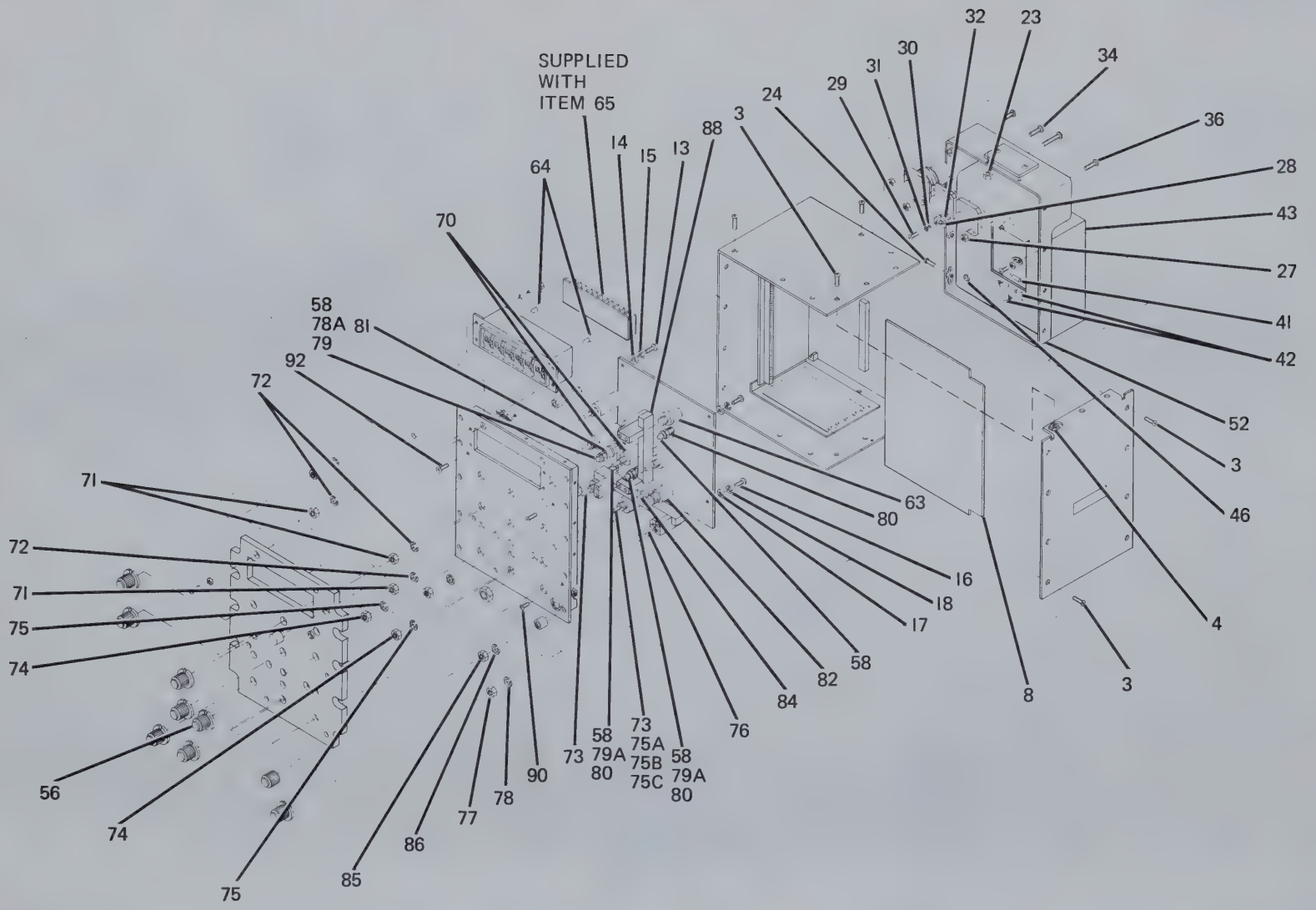

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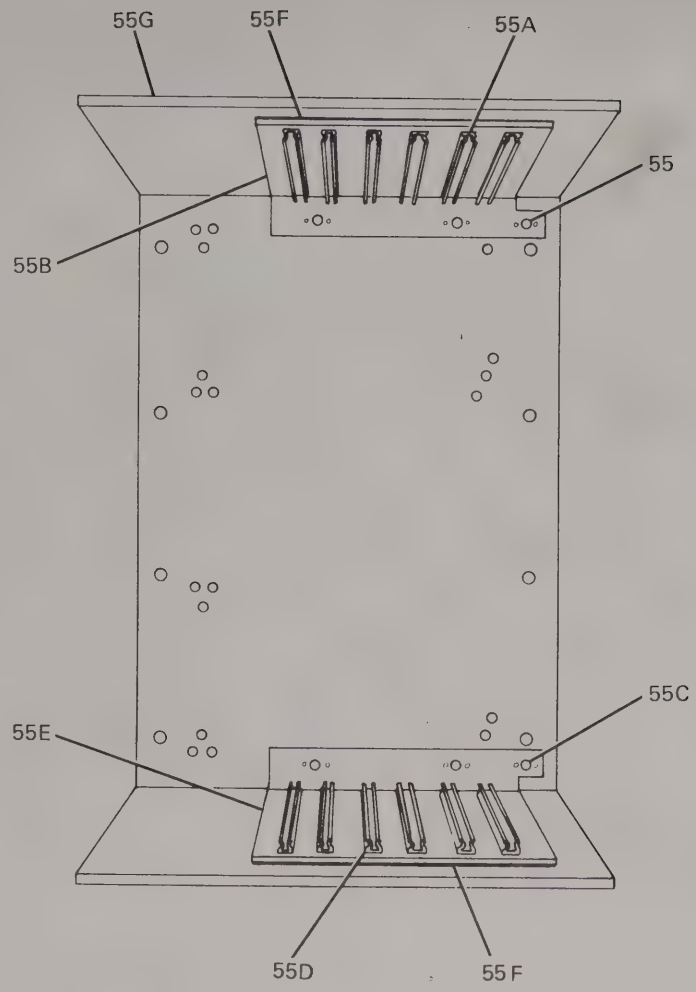
Figure 6-13. Receive Control Head A8 (Sheet 2 of 3)



DETAIL A

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Figure 6-13. Receive Control Head A8 (Sheet 3 of 3)

FIGURE AND INDEX NO.	PART NUMBER	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
13	787-6444-001	HEAD, RECEIVE CONTROL C-8362/TSC-60V /SEE FIGURE 1 FOR NHA/ . . .	REF	
- 1	795-8764-001	. NAMEPLATE /EFF TO REV LTR U/.	1	
- 1	795-8764-001	. NAMEPLATE /EFF WITH REV LTR U/.	1	
		-ATTACHING PARTS-		
	330-4025-020	. SCREW, TAPPING, SST, 2-56 X 3/16 /45722/ /330-4025-020/ . . . . /REPLACE WITH P/N MS24630-2/	2	
	MS24630-2	. SCREW	REF	
		---*---		
- 2	280-3035-000	. LABEL, INSTR /16319/ /280-3035-000/ /EFF TO CI-72357/	1	
- 2	280-1339-010	. LABEL, INSTR /16319/ /280-1339-000/ /EFF WITH CI-72357/	1	
	789-2640-002	. COVER, CARD CAGE.	1	
		-ATTACHING PARTS-		
- 3	MS24693C25	. SCREW /342-1350-160/.	12	
		---*---		
- 4	NAS1068A06	. . NUT /333-0888-000/.	4	
- 5	789-2639-002	. . COVER	1	
	607-2418-001	. CONNECTOR, STRAPPING.	1	
- 6	372-2255-020	. . CONTACT, ELECTRICAL	14	
- 7	372-2626-045	. . HOUSING, CONNECTOR.	AR	
- 8	793-9260-001	. CARD, LOGIC LEVEL SLAVE /SEE FIGURE 3 FOR BREAKDOWN/.	1	
- 9	789-2612-001	. CARD, MATRIX /SEE FIGURE 9 FOR BREAKDOWN/	1	
		-ATTACHING PARTS-		
- 10	MS51957-14	. SCREW /343-0134-000/.	1	
- 11	DIE845	. WASHER, FLAT, SST, 0.119 ID X 0.218 OD /72606/ /310-0460-000/ .	1	
- 12	310-0278-000	. WASHER, LOCK, SST, 0.115 ID X 0.202 OD /70318/ /310-0278-000/ .	1	
- 13	MS51957-18	. SCREW /343-0138-000/.	2	
- 14	DIE845	. WASHER, FLAT, SST, 0.119 ID X 0.218 OD /72606/ /310-0460-000/ .	2	
- 15	310-0278-000	. WASHER, LOCK, SST, 0.115 ID X 0.202 OD /70318/ /310-0278-000/ .	2	
- 16	MS51957-4	. SCREW /343-0125-000/.	4	
- 17	310-6320-000	. WASHER, FLAT, SST, 0.092 ID X 0.218 OD /79807/ /310-6320-000/ .	4	
- 18	310-0070-000	. WASHER, LOCK, SST, 0.097 ID X 0.165 OD /79807/ /310-0070-000/ .	4	
		---*---		
	795-5243-001	. CONNECTOR, ADDRESS STRAPPING.	1	
- 19	JTG06A14-37P014	. . CONNECTOR, PLUG, ELEC /77820/ /371-9007-110/.	1	
	795-5245-001	. . SHIELD ASSEMBLY	1	
- 20	10-352421-14	. . . ADAPTER, THREADED RING /77820/ /371-9006-390/	1	
- 20A	789-2667-001	. . . COVER, CONNECTOR.	1	
- 21	789-2666-001	. HOLDDOWN, CONNECTOR	2	
		-ATTACHING PARTS-		
	MS51957-21	. SCREW /343-0141-000/.	2	
	DIE845	. WASHER, FLAT, SST, 0.119 ID X 0.218 OD /72606/ /310-0460-000/ .	2	
		---*---		
	789-2593-001	. PANEL ASSEMBLY, REAR.	1	
		-ATTACHING PARTS-		
- 22	MS24693C24	. SCREW /342-1350-150/.	4	
- 23	P313-0045-000	. NUT, PLAIN, HEX, SST, 6-32 /77250/ /313-0045-000/	4	
- 24	MS24693C25	. SCREW /342-1350-160/.	4	
		---*---		
- 25	JTP02RE16-55P014	. . CONNECTOR, RCPT, ELEC /77820/ /359-0609-260/.	1	
		-ATTACHING PARTS-		
- 26	MS51957-15	. . SCREW /343-0135-000/.	4	
- 27	68NM40	. . NUT, SLFLKG, HEX, AL, 4-40 /72962/ /333-0347-000/	4	
		---*---		
- 28	HP8N	. . CLAMP, LOOP /09922/ /150-1545-000/.	1	
		-ATTACHING PARTS-		
- 29	MS51957-14	. . SCREW /343-0134-000/.	1	
		---*---		
- 30	310-6340-000	. . WASHER, FLAT, SST, 0.125 ID X 0.281 OD /79807/ /310-6340-000/	1	
- 31	310-0278-000	. . WASHER, LOCK, SST, 0.115 ID X 0.202 OD /70318/ /310-0278-000/	1	
- 32	540-9176-003	. . POST.	1	
- 33	JTP02RE12-98P014	. . CONNECTOR, RCPT, ELEC /77820/ /359-0609-110/.	1	
		-ATTACHING PARTS-		
- 34	MS51957-15	. . SCREW /343-0135-000/.	3	
- 35	68NM40	. . NUT, SLFLKG, HEX, AL, 4-40 /72962/ /333-0347-000/	3	
- 36	MS51957-16	. . SCREW /343-0136-000/.	1	
- 37	MS35649-244	. . NUT /313-0043-000/.	1	
		---*---		
- 38	JTP02RE14-37S014	. . CONNECTOR, RCPT, ELEC /77820/ /359-0607-160/.	1	
		-ATTACHING PARTS-		
- 39	MS51957-15	. . SCREW /343-0135-000/.	4	
- 40	68NM40	. . NUT, SLFLKG, HEX, AL, 4-40 /72962/ /333-0347-000/	4	
		---*---		
- 41	RW69V101	. . RESISTOR /747-5340-000/	1	
- 42	RE65G10R0	. . RESISTOR /747-8954-000/	2	
		-ATTACHING PARTS-		
	MS51959-4	. . SCREW /342-0134-000/.	4	
	310-0070-000	. . WASHER, LOCK, SST, 0.097 ID X 0.165 OD /79807/ /310-0070-000/	4	
	MS35649-224	. . NUT /313-0037-000/.	4	
		---*---		
- 43	793-9305-001	. . POWER SUPPLY /SEE FIGURE 10 FOR BREAKDOWN/.	1	
		-ATTACHING PARTS-		
- 44	MS51957-43	. . SCREW /343-0187-000/.	1	
- 45	MS35333-72	. . WASHER /373-0003-000/	1	
- 46	MS51957-42	. . SCREW /343-0186-000/.	3	
	MS35333-72	. . WASHER /373-0003-000/	3	
		---*---		
- 47	2104-08-02-2520N	. . TERMINAL, LUG /78189/ /304-0319-000/.	1	
	795-8759-001	. . CABLE ASSEMBLY.	1	
- 48	372-2255-010	. . . CONTACT, ELECTRICAL	8	
- 48A	372-2255-020	. . . CONTACT, ELECTRICAL	58	

FIGURE AND INDEX NO.	PART NUMBER	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
13 - 48B	SSTINAT	. . . STRAP, CABLE /06383/ /150-0681-050/ /EFF TO REF LTR F/	100	
- 48B	MS3367-4-9	. . . TIE, CABLE 7435-1169-100/ /EFF WITH REV LTR F/.	100	
- 49	TF300	. . TERMINAL, STUD /98291/ /306-1018-000/	2	
		-ATTACHING PARTS-		
	MS51959-1	. . SCREW /342-0131-000/ /EFF TO REV LTR U/	2	
	MS51959-2	. . SCREW /342-0132-000/ /EFF WITH REV LTR U/	2	
		---*---		
	624-9726-001	. . CONNECTOR	1	
- 50	372-2626-57	. . . HOUSING	1	
	789-2658-047	. . PANEL, REAR, FABRICATED	1	
- 51	NAS1068A06	. . . NUT /333-0888-000/.	8	
		-ATTACHING PARTS-		
	MS20426AD2-3	. . . RIVET /305-1352-000/.	16	
		---*---		
- 52	789-2588-002	. . . PANEL, REAR	1	
	789-2626-001	. CARD BACKPLANE.	1	
		-ATTACHING PARTS-		
	MS51957-14	. SCREW /343-0134-000/ /EFF TO REV LTR W/	4	
	302-4800-000	. WASHER, NM FBR, 0.116 ID X 1/4 OD /74921/ . . . . . /302-4800-000/ /EFF WITH REV LTR W/	4	
	DIE845	. WASHER, FLAT, SST, 0.119 ID X 0.218 OD /72606/. . . /310-0460-000/	4	
		---*---		
- 53	768-5919-003	. . PIN, POLARIZING	6	
- 53A	372-2601-045	. . CONTACT, ELECTRICAL	373	
- 53B	600-9276-011	. . BACKPLANE, FAB.	1	
		. CAGE, CARD.	1	
		-ATTACHING PARTS-		
- 54	MS24693C25	. SCREW /342-1350-160/.	10	
		---*---		
	789-2657-001	. . GUIDE ASSEMBLY, UPPER	1	
		-ATTACHING PARTS-		
	MS20426AD2-4	. . RIVET /305-1353-000/.	9	
		---*---		
- 55	LHTA57M2860-40	. . NUTPLATE, 4-40 /72962/ /333-1449-010/	3	
		-ATTACHING PARTS-		
	MS2C426AD2-3	. . . RIVET /305-1352-000/.	6	
		---*---		
- 55A	775-466C-007	. . GUIDE CARD, GRIP.	6	
- 55B	789-2656-001	. . . GUIDE, PLATE.	1	
	789-2636-001	. . GUIDE ASSEMBLY, LOWER	1	
		-ATTACHING PARTS-		
	MS20426AD2-4	. . RIVET /305-1353-00/	9	
		---*---		
- 55C	LHTA57M2860-40	. . NUT PLATE, 4-40 /72962/ /333-1449-010/.	3	
		-ATTACHING PARTS-		
	MS20426AD2-3	. . . RIVER /305-1352-000/.	6	
		---*---		
- 55D	775-4660-007	. . GUIDE CARD, GRIP.	6	
- 55E	789-2597-001	. . . GUIDE, PLATE.	1	
- 55F	795-5246-001	. . SHIELD, KNITTED MESH.	2	
- 55G	789-2641-001	. . FRAME, CARD CAGE.	1	

FIGURE AND INDEX NO	PART NUMBER	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
- 56	MS91528-OH1B	. KNOB /281-0188-040/	8	
- 57	MS91528-001B	. KNOB /281-0386-000/ /EFF TO REV LTR V/.	1	
- 57	633-4510-001	. KNOB /EFF WITH REV LTR W/	1	
- 58	MS24515-685	. LAMP, INCANDESCENT /17537//262-2204-060/	4	
- 59	381	. LAMP, INCANDESCENT /24455//262-2113-000/	1	
- 59A	183-1474-001	. . LENS, CAP /72619/	1	
- 60	789-2583-005	. PANEL, ILLUMINATED.	1	
		-ATTACHING PARTS-		
- 61	P343-0035-000	. SCREW, MACH, SST, 6-32 X 7/16 /77250/ . /343-0035-000/	6	
- 62	759-4321-001	. MASTER, SHOCK	6	
		---*---		
	789-2591-001	. PANEL ASSEMBLY, FRONT	1	
- 63	183-0101-1474-60	. . SWITCH, PUSH /72619/ /266-7086-170/	1	
- 64	MS24515-685	. . LAMP, INCANDESCENT /17537/. . . . . /262-2204-060/	6	
- 65	7C63	. . SWITCH, RTRY /07125/ /259-9590-030/ .	1	
		-ATTACHING PARTS-		
- 66	MS51959-3	. . SCREW /342-0133-000//EFF TO REV LTR U/	4	
	MS51959-4	. . SCREW /342-0134-000//EFF WITH REV LTR U/	4	
- 67	310-6320-000	. . WASHER, FLAT, SST, 0.092 ID X 0.218 OD /79807/ /310-6320-000/	4	
- 68	310-0070-000	. . WASHER, LOCK, SST, 0.097 ID X 0.165 OD /79807/ /310-0070-000/	4	
- 69	MS35649-224	. . NUT /313-0037-000/.	4	
		---*---		
- 70	259-2769-060	. . SWITCH, RTRY /259-2769-060/	5	
		-ATTACHING PARTS-		
- 71	P334-0287-00	. . NUT, PLAIN, HEX, SST, 1/4-32 /77250/. /334-0287-000/	5	
- 72	1214-05CDPL	. . WASHER, LOCK, STL, 0.267 ID X 0.408 OD /78189/ /373-0151-000/	5	
		---*---		
- 73	259-2769-020	. . SWITCH, RTRY /259-2769-020/	2	
		-ATTACHING PARTS-		
- 74	P334-0287-00	. . NUT, PLAIN, HEX, SST, 1/4-32 /77250/. /344-0287-000/	2	
- 75	121405CDPL	. . WASHER, LOCK, STL, 0.267 ID X 0.408 OD /78189/ /373-0151-000/	2	
		---*---		
	795-8758-001	. . CABLE ASSEMBLY.	1	
- 75A	372-2255-010	. . . CONTACT, ELECTRICAL	3	
- 75B	372-2255-020	. . . CONTACT, ELECTRICAL	55	
- 75C	SSTINAT	. . . STRAP, CABLE /06383/150-0681-050/ . /EFF TO REV LTR K/	100	
	MS3367-4-9	. . . TIE, CABLE /435-1169-100/ /EFF WITH REF LTR K/	100	
- 76	259-2769-010	. . SWITCH, RTRY /259-2769-010/	1	
		-ATTACHING PARTS-		

FIGURE AND INDEX NO	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
13 - 77	P334-0287-00	. . NUT, PLAIN, HEX, SST, 1/4-32 /77250/ /334-0287-000/	1	
- 78	1214-05CDPL	. . WASHER, LOCK, STL, 0.267 ID X 0.408 OD /78189/ /373-0151-000/	1	
		---*---		
- 78A	160A604RED	. . LENS /72765/ /262-2322-140/	1	
- 79	5160-458-604RED	. . LIGHT, IND /72765/ /262-2322-070/	1	
- 79A	160A604GRN	. . LENS /72765/ /262-2322-130/	3	
- 80	5160-458-604GRN	. . LIGHT, IND /72765/ /262-2322-060/	3	
- 81	130GOLD	. . CONNECTOR, RCPT, ELEC /04211/ /372-2225-010/.	1	
- 82	W1046	. . SWITCH, PUSH /81640/ /266-2701-020/ /EFF TO REV LTR U/. . . .	1	
- 82	W1046CE	. . SWITCH, PUSH /81640/ /266-2701-060/ /EFF WITH REV LTR U/. . .	1	
		-ATTACHING PARTS-		
- 83	318-0035	. . NUT, PLAIN, RD, BRS, 1/2-32 /97564/ /334-2736-020/.	1	
		/EFF WITH REV LTR U/		
- 83		DELETED /EFF WITH REV LTR U/		
		---*---		
- 84	M22-01-C0091SB	. . RESISTOR /749-4727-030/	1	
		-ATTACHING PARTS-		
- 85	P334-0287-00	. . NUT, PLAIN, HEX, STL, 1/4-32 /77250/ /334-0287-000/	1	
		/EFF TO REV LTR L/		
- 85		DELETED /EFF WITH REV LTR L/		
- 86	1214-05CDPL	. . WASHER, LOCK, STL, 0.267 ID X 0.408 OD /78189/ /373-0151-000/	1	
		---*---		
- 87	789-2653-001	. . CONNECTOR, NO. 2.	1	
		-ATTACHING PARTS-		
	MS51957-9	. . SCREW /343-0129-000/.	2	
	310-6320-000	. . WASHER, FLAT, SST, 0.092 ID X 0.218 OD /79807/ /310-6320-000/	2	
	68NM26	. . NUT, SLFLKG, HEX, AL, 2-56 /72962/ /333-0327-000/	2	
		---*---		
- 88	789-2652-001	. . CONNECTOR, NO 1	1	
		-ATTACHING PARTS-		
	MS51957-9	. . SCREW /343-0129-000/.	2	
	310-6320-000	. . WASHER, FLAT, SST, 0.092 ID X 0.218 OD /79807/ /310-6320-000/	2	
	68NM26	. . NUT, SLFLKG, HEX, AL, 2-56 /72962/ /333-0327-000/	2	
		---*---		
- 89	789-2590-001	. . POST, CONNECTOR MOUNTING.	4	
		-ATTACHING PARTS-		
- 90	MS51959-14	. . SCREW /342-0045-000/.	8	
		---*---		
- 91	789-2637-001	. . POST, HEX	3	
		-ATTACHING PARTS-		
- 92	MS51959-14	. . SCREW /342-0045-000/.	3	
		---*---		
	789-2587-001	. . PANEL, FRONT, MOUNTING, RECEIVER.	1	
		PARTIAL BREAKDOWN FOLLOWS		
- 93	MAS1068A06	. . . NUT PLATE /333-0888-000/.	14	
		-ATTACHING PARTS-		
	MS20426AD2-3	. . . RIVET /305-1352-000/.	28	
		---*---		
- 94	LHTA51M2860-62	. . . NUT PLATE, SLFLKG, SST, 6-32 /72962/ /333-1157-000/	2	
		/REPLACE WITH P/N NAS697C06/		
	NAS697CC6	. . . NUT PLATE	REF	
		-ATTACHING PARTS-		
- 95	MS20426AD2-3	. . . RIVET /305-1352-000/.	4	
		---*---		
- 96	MRPN6-32SCL	. . . NUT, PPSD, CD PL STL, 6-32 /83324/ /334-2615-000/	4	
- 97	793-6249-001	. . . BUSHING, INDICATOR LIGHT.	4	
- 98	PFSC3 1-2 38	. . . STUD ASSY /72794/ /012-0003-010/.	10	
- 99	789-2679-001	. . . PANEL, FABRICATED	1	

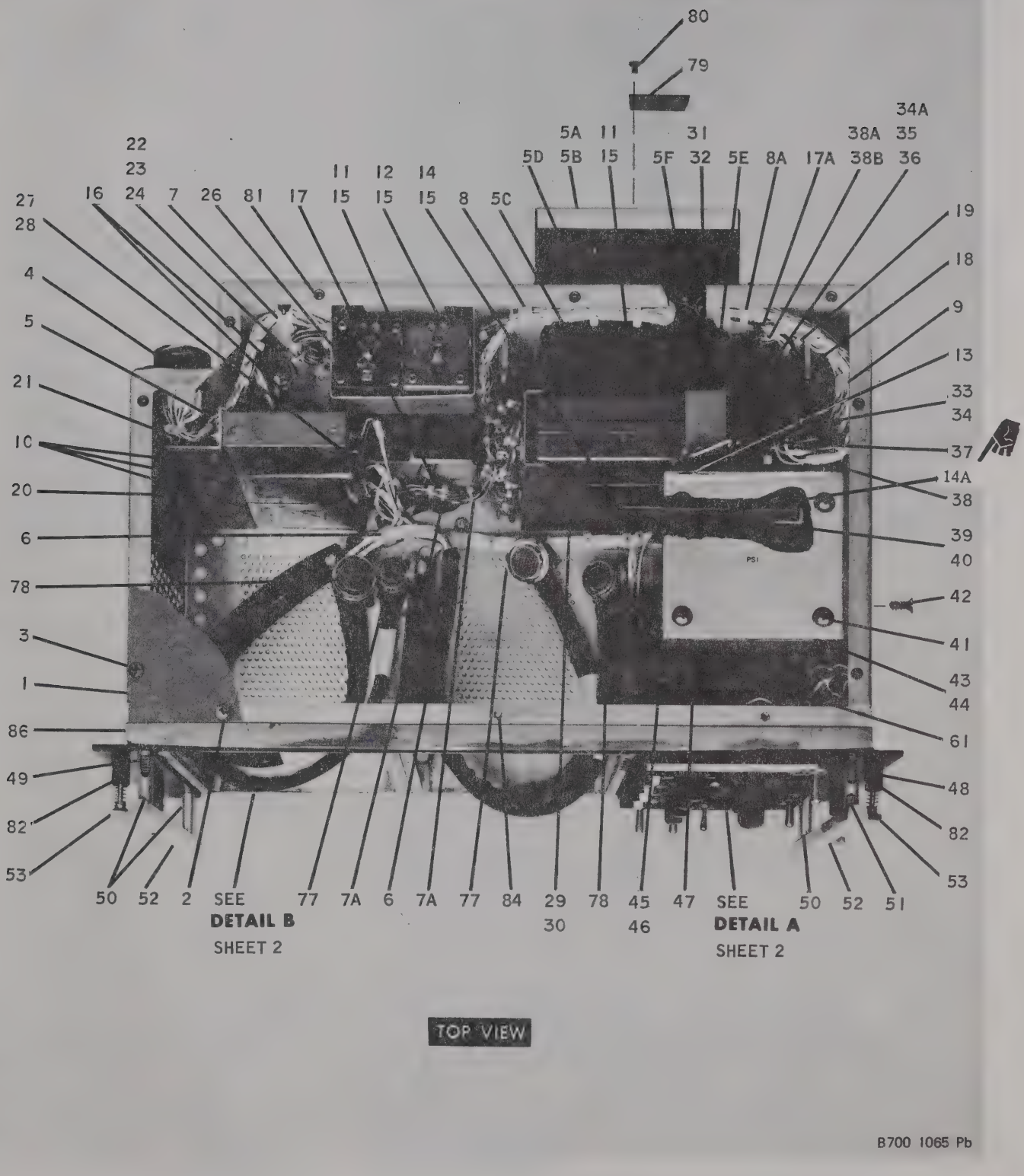

Figure 6-14. Audio Control Unit (Sheet 1 of 2)

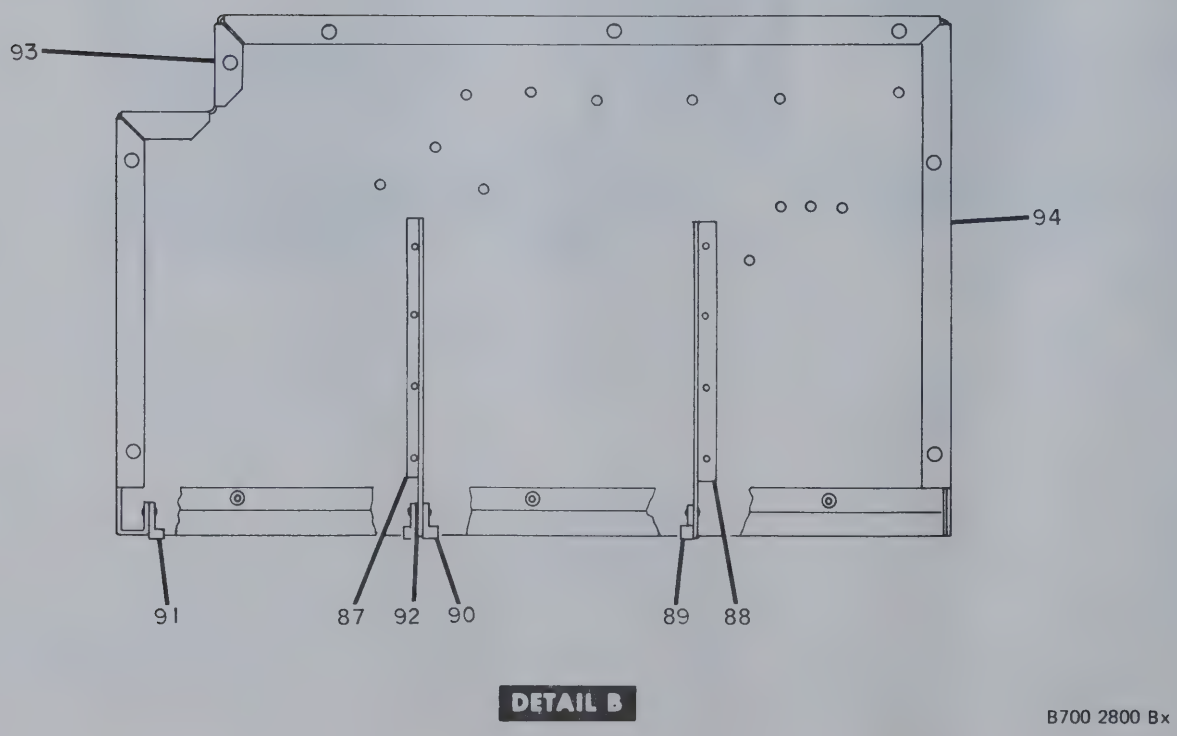

Figure 6-14. Audio Control Unit (Sheet 2 of 2)

FIGURE AND INDEX NO.	PART NUMBER	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
14	789-8117-001	UNIT, AUDIO CONTROL, C-8364/TSC-60LV/ /SEE FIGURE 1 FOR NHA/. . .	REF	
- 1	793-6044-001	. COVER, AUDIO CONTROL.	1	
		-ATTACHING PARTS-		
- 2	MS51957-24	. SCREW /343-0165-000/.	3	
- 3	MS51957-28	. SCREW /343-0169-000/.	8	
		---*---		
- 4	MS3112E22-55P	. CONNECTOR /371-6650-000/.	1	
		-ATTACHING PARTS-		
	MS51957-4	. SCREW /343-0125-000/.	4	
	310-6320-000	. WASHER, FLAT, 0.092 ID X 0.218 OD /79807/ /310-6320-000/. . .	4	
	MS35338-134	. WASHER /310-0275-000/	4	
	MS35649-224	. NUT /313-0037-000/.	4	
		---*---		
- 5	MS3102R10SL3P	. CONNECTOR /357-3408-000/.	1	
		-ATTACHING PARTS-		
	MS51957-4	. SCREW /343-0125-000/.	4	
	310-6320-000	. WASHER, FLAT, 0.092 ID X 0.218 OD /79807/ /310-6320-000/. . .	4	
	MS35338-134	. WASHER /310-0275-000/	4	
	MS35649-224	. NUT /313-0037-000/.	4	
		---*---		
- 5A	616-7292-001	. BRACKET, FAN.	1	
		-ATTACHING PARTS		
	MS51957-28	SCREW /343-0169-000/.	4	
	310-0046-000	WASHER, FLAT, SST, 0.147 ID X 0.312 OD /79807/ /310-0046-000/ .	4	
	MS35338-136	WASHER /310-0282-000/	4	
	P313-0045-000	NUT, PLAIN, HEX, SST, 6-32 /77250/ /313-0045-000/	4	
		---*---		
- 5B	616-7291-001	FILTER, FAN	1	
- 5C	616-7289-001	SCREEN, FILTER.	2	
- 5D	A086312	. FAN, TUBEAXIAL, 50 TO 400 HZ /82877/ /009-0172-010/	1	
		-ATTACHING PARTS-		
	MS51957-28	. SCREW /343-0169-000/.	4	
	310-0046-000	. WASHER, FLAT, SST, 0.147 ID X 0.312 OD /79807/ /310-0046-000/ .	4	
	MS35338-136	. WASHER /310-0282-000/	4	
	P313-0045-000	. NUT, PLAIN, HEX, SST, 6-32 /77250/ /313-0045-000/	4	
		---*---		
- 5E	616-7290-001	. GASKET, RFI	1	
- 5F	MS35489-4	. GROMMET, RUBBER /201-0001-000/.	1	
- 6	HP10N	. CLAMP, LOOP /09922/ /150-1546-000/.	2	
		-ATTACHING PARTS-		
	MS51959-28	. SCREW /342-0062-000/.	2	
	310-0046-000	. WASHER, FLAT, SST, 0.147 ID X 0.312 OD /79807/ /310-0046-000/ .	2	
	MS35338-136	. WASHER /310-0282-000/	2	
	P313-0045-000	. NUT, PLAIN, HEX, SST, 6-32 /77250/ /313-0045-000/	2	
		---*---		
- 7	HP4N	. CLAMP, LOOP /09922/ /150-1541-000/ /EFF TO REV LTR AF/. . . .	1	
- 7	HP5N	. CLAMP, LOOP /09922/ /150-1542-000/ /EFF WITH REV LTR AF/. . .	1	
		-ATTACHING PARTS-		
	MS51957-28	. SCREW /343-0169-000/.	1	
	310-0046-000	. WASHER, FLAT, SST, 0.147 ID X 0.312 OD /79807/ /310-0046-000/ .	1	
	MS35338-136	. WASHER /310-0282-000/	2	
	P313-0045-000	. NUT, PLAIN, HEX, SST, 6-32 /77250/ /313-0045-000/	1	
		---*---		
- 7A	HP8N	. CLAMP, LOOP /09922/ /150-1545-000/ /EFF WITH REV LTR AF/. . .	2	
		-ATTACHING PARTS-		
	MS51959-28	. SCREW /342-0062-000/ /EFF WITH REV LTR AF/.	2	
	310-0046-000	. WASHER, FLAT, SST, 0.147 ID X 0.312 OD /79807/ /310-0046-000/ .	2	
		/EFF WITH REV LTR AF/		
	MS35338-136	. WASHER /310-0282-000/ /EFF WITH REV LTR AF/	2	
	P313-0045-000	. NUT, PLAIN, HEX, SST, 6-32 /77250/ /313-0045-000/ /EFF WITH . .	2	
		REV LTR AF/		
		---*---		
- 8	HP7N	. CLAMP, LOOP /09922/ /150-1544-000/ /EFF TO REV LTR AF/. . . .	1	
- 8	HP6N	. CLAMP, LOOP /09922/ /150-1543-000/ /EFF WITH REV LTR AF/. . .	1	
		-ATTACHING PARTS-		
	MS51957-28	. SCREW /343-0169-000/ /EFF TO REV LTR AF/.	1	
	MS51957-30B	. SCREW /343-0036-000/ /EFF WITH REV LTR AF/		
	310-0046-000	. WASHER, FLAT, SST, 0.147 ID X 0.312 OD /79807/ /310-0046-000/ .	1	
	MS35338-136	. WASHER /310-0282-000/	1	
	P313-0045-000	. NUT, PLAIN, HEX, SST, 6-32 /77250/ /313-0045-000/	1	
		---*---		
- 8A	HP6N	. CLAMP, LOOP /09922/ /150-1543-000/ /EFF WITH REV LTR AF/. . .	1	
		-ATTACHING PARTS-		
	MS51957-30B	. SCREW /343-0036-000/ /EFF WITH REV LTR AF/.	1	
	310-0046-000	. WASHER, FLAT, SST, 0.147 ID X 0.312 OD /79807/ /310-0046-000/ .	1	
		/EFF WITH REV LTR AF/		
	MS35338-136	. WASHER /310-0282-000/ /EFF WITH REV LTR AF/	1	
	P313-0045-000	. NUT, PLAIN, HEX, SST, 6-32 /77250/ /313-0045-000/ /EFF WITH REV	1	
		LTR AF/		
		---*---		
- 9	HP8N	. CLAMP, LOOP /09922/ /150-1545-000/ /EFF TO REV LTR AF/. . . .	1	
- 9	HP7N	. CLAMP, LOOP /09922/ /150-1544-000/ /EFF WITH REV LTR AF/. . .	1	
		-ATTACHING PARTS-		
	MS51959-28	. SCREW /342-0062-000/.	1	
	310-0046-000	. WASHER, FLAT, SST, 0.147 ID X 0.312 OD /79807/ /310-0046-000/ .	1	
	MS35338-136	. WASHER /310-0282-000/	1	
	P313-0045-000	. NUT, PLAIN, HEX, SST, 6-32 /77250/ /313-0045-000/	1	
		---*---		
- 10	JW33-1114A	. FILTER, RF /56289/ /241-8041-010/	3	

FIGURE AND INDEX NO	PART NUMBER	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
14 - 11	TLC333C	. AMPLIFIER. AF /93663/ /270-0089-010/ /EFF WITH REV LTR AF/	2	
- 12	TLC555C	. AMPLIFIER. AF /93663/ /270-0091-010/	1	
- 13	TLC444C	. AMPLIFIER. AF /93663/ /270-0088-010/	1	
- 14	TLC213MOD	. AMPLIFIER. AF /64294/ /270-0090-010/	1	
- 14A	TLC444			
- 15	78S11M1005	. SOCKET, TUBE /02660/ /372-1952-000/	5	
- 16	4JK14	. FILTER, LP /56289/ /241-0303-000/.	2	
- 17	2104-06-02-252ON	. LUG, TERMINAL /78189/ /304-0318-000/	8	
		-ATTACHING PARTS-		
	MS51957-28	. SCREW /343-0169-000/	1	
	MS51959-28	. SCREW /342-0062-000/	3	
	310-0046-000	. WASHER, FLAT, SST, 0.147 ID X 0.312 OD /79807/ /310-0046-000/	3	
	MS35338-136	. WASHER /310-0282-000/	4	
	P313-0045-000	. NUT, PLAIN, HEX, SST, 6-32 /77250/ /313-0045-000/	4	
		---*---		
- 17A	3340	. TERMINAL, STUD /17117/ /306-2519-030/	3	
		-ATTACHING PARTS-		
	P347-0032-000	. SCREW, MACHINE, SST, 6-32 X 3/16 IN. LG /77250/ /347-0032-000/ /EFF TO REV LTR AF/	3	
	MS51957-26	. SCREW /343-0167-000/ /EFF WITH REV LTR AF/. .	3	
	MS35338-136	. WASHER /310-0282-000/	3	
		---*---		
- 18	540-9225-003	. POST, HEX	2	
		-ATTACHING PARTS-		
	MS51957-28	. SCREW /343-0169-000/.	4	
	310-0046-000	. WASHER, FLAT, SST, 0.147 ID X 0.312 OD /79807/ /310-0046-000/	6	
	MS35338-136	. WASHER /310-0282-000/	4	
		---*---		
- 19	783-1427-001	. CARD, AUDIO CONTROL /SEE FIGURE IS FOR BREAKDOWN/	1	
	793-5961-001	. BRACKET, SIGNAL FILTER.	1	
		-ATTACHING PARTS-		
	MS51959-29	. SCREW /342-0063-000/.	3	
		---*---		
- 20	FPN6-32SCL	. . NUT, PRESS, CO PL STL, 6-32 /83324/ /334-1152-000/	3	
- 21	793-5960-002	. BRACKET, FABRICATED	1	
	793-5990-001	. BRACKET, POWER FILTER	1	
		-ATTACHING PARTS-		
	MS51957-29	. SCREW /343-0170-000/.	2	
		---*---		
- 22	FPN6-325SCL	. . NUT, PRESS, CD PL STL, 6-32 /83324/ /334-1152-000/	2	
- 23	793-5989-002	. BRACKET, FABICATED.	1	
- 24	796-1260-001	. SPACER, PLATE	1	
	793-5981-001	. BRACKET, AMPLIFIER.	1	
		-ATTACHING PARTS-		
	MS51959-29	. SCREW /342-0063-000/.	2	
		---*---		
- 25	FPN6-32SCL	. . NUT, PRESS, CD PL STL, 6-32 /83324/ /334-1152-000/	2	
- 26	793-5980-002	. . BRACKET, FABRICATED	1	
	793-5994-001	. RETAINER, AMPLIFIER	1	

FIGURE AND INDEX NO.	PART NUMBER	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
14 -		-ATTACHING PARTS-		
- 26	MS51957-29	. SCREW /343-0170-000/	2	
		---*---		
- 27	FPN6-32SCL	. . NUT, PRESS, CD PL STL, 6-32 /83324/. . . . . /334-1152-000/	2	
- 28	793-5993-002	. . RETAINER, FABRICATED	1	
	793-5988-001	. BRACKET, AMPLIFIER	1	
		-ATTACHING PARTS-		
	MS51959-29	. SCREW /342-0063-000/	4	
		---*---		
- 29	FPN6-32SCL	. . NUT, PRESS, CO PL STL, 6-32 /83324/. . . . . /344-1152-000/	4	
- 30	793-5987-002	. . BRACKET, AMPLIFIER..	1	
	793-6001-001	. BRACKET, AMPLIFIER.	1	
		-ATTACHING PARTS-		
	MS51959-29	. SCREW /342-0063-000/	2	
		---*---		
- 31	FPN-32SCL	. . NUT, PRESS, CD PL STL, 6-32 /83324/. . . . . /344-1152-000/	2	
- 32	793-6000-002	. . BRACKET, FABRICATED.	1	
	793-5964-001	. BRACKET, CARD.	2	
		-ATTACHING PARTS-		
	MS51959-29	. SCREW /342-0063-000/..	4	
		---*---		
- 33	FPN6-32SCL	. . NUT, PRESS, CD PL STL, 6-32 /83324/. . . . . /334-1152-000/	3	
- 34	793-5956-002	. . BRACKET, FABRICATED.	1	
- 34A	M21097-9-01	. CONTACT, ELECTRICAL.	172	
- 35	456-01-25-788	. KEY, CONNECTOR /71785/ /372-7348-000/.	1	
- 36	M21097-8-4	. CONNECTOR /372-7331-000/	1	
		-ATTACHING PARTS-		
	MS51957-17	. SCREW /343-0137-000/	2	
	310-6340-000	. WASHER, FLAT, SST, 0.125 ID X 0.281 OD /78907/ . /310-6340-0007/	4	
	MS35338-135	. WASHER /310-0279-000/.	2	
	P313-0132-000	. NUT, PLAIN, HEX, SST, 4-40 /77250/ . . . . . /313-0132-000/	2	
		---*---		
- 37	41170	. TERMINAL, LUG /0079/ /304-1256-000/.	31	
- 38	37TBB	. BOARD /367-1434-000	1	
		-ATTACHING PARTS-		
	MS51597-31	. SCREW /343-0173-000/ /EFF TO REV LTR AF/	4	
	MS51957-30	. SCREW /343-0172-000/ /EFF WITH REV LTR AF/ . . .	4	
	P313-0045-000	. NUT, PLAIN, HEX, SST, 6-32 /77250/ . . . . . /313-0045-000/	4	
		---*---		
- 38A	CPO9A1KC224K3	. CAPACITOR /962-0755-000/	1	
- 38B	100-200-9-23	. HOLDER, COMPONENT /99378/ /139-2234-000/	1	
		-ATTACHING PARTS-		

FIGURE ON INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
14	MS51957-4	. SCREW /343-0125-000/.	2	
	310-6320-000	. WASHER, FLAT, SST, 0.092 ID X 0.218 OD .79807/. . /310-6320-000/	2	
	MS35228-134	. WASHER /310-0275-000/	2	
	MS35649-224	. NUT /313-0037-000/.	2	
		---*---		
	793-5998-001	. BRACKET, AMPLIFIER.	1	
		-ATTACHING PARTS-		
	MS51959-29	. SCREW /342-0063-000/.	1	
		---*---		
- 39	FPN6-32SCL	. . NUT, PRESS, CD PL STL, 6-32 /83324/ /334-1152-000/	1	
- 40	793-5997-002	. . BRACKET, FABRICATED	1	
	793-5958-001	. BRACE, UPPER POWER SUPPLY	1	
		-ATTACHING PARTS-		
- 41	MS51958-63	. SCREW /343-0228-000/.	4	
	310-0049-000	. WASHER. FLAT. SST, 0.203 ID X 0.500 OD /79807/. . /310-0049-000/	4	
	310-0073-000	. WASHER, LOCK, SST, 0.194 ID X 0.323 OD /79807/. . /310-0073-000/	4	
- 42	MS51959-29	. SCREW /342-0063-000/.	3	
		---*---		
- 43	FPN6-32SCL	. . NUT, PRESS, CD PL STL, 6-32 /83324/ /334-1152-000/	3	
- 44	793-5957-002	. . BRACE, FABRICATED	1	
	793-5950-001	. BRACKET, LOWER POWER SUPPLY	1	
		-ATTACHING PARTS-		
	MS51959-29	. SCREW /342-0063-000/.	4	
	310-0049-000	. WASHER, FLAT, SST, 0.203 ID X 0.500 OD /79807/. . /310-0049-000/	4	
	310-0073-000	. WASHER, LOCK, SST, 0.194 ID X 0.323 OD /79807/. . /310-0073-000/	4	
	MS35650-304	. NUT /313-0019-000/.	4	
		---*---		
- 45	FPN6-32SCL	. . NUT, PRESS, CD PL STL, 6-32 /83324/ /334-1152-000/	4	
- 46	793-5949-002	. . BRACKET, FABRICATED	1	
- 47	PM23-3-0-750A	. POWER SUPPLY /13850/ /270-0101-0101/.	1	
- 48	MS51960-64	. SCREW /342-0223-000/.	2	
- 49	MS51958-63	. SCREW /343-0228-000/.	2	
- 50	763-3341-001	. POST, HANDLE.	4	
- 51	763-3340-001	. STUD, HANDLE.	4	
- 52	763-3339-003	. HANDLE, PANEL	2	
- 53	H538-30-10	. FASTENER, CAPTIVE /82014/ /012-4958-080/.	4	
- 54	MS24515-685	. LAMP /262-0934-000/	5	
- 54A	160A604WHT	. . LENS /72765/ /262-2322-110/	4	
- 55	5160-458-604WHT	. LAMPHOLDER /72765/ /262-2322-040/	4	
- 55A	160A604GRN	. . LENS /72765/ /262-2322-130/	1	
- 56	5160-458-604GRN	. LAMPHOLDER /72765/ /262-2322-060/	1	
- 57	MS91528-OH18	. KNOB /281-0188-040/	4	
		-ATTACHING PARTS-		
	MS51963-9	. SETSCREW /328-5020/000/	8	
		---*---		
- 58	259-2641-020	. SWITCH, RTRY /259-2641-020/	4	
- 59	MS91528-0018	. KNOB /281-0386-000/	1	
- 60	749-4728-050	. RESISTOR, VAR, 15K, 10%, 12.5W /44655/ /749-4728-050/	1	
		-ATTACHING PARTS-		
	P334-0287-000	. NUT, PLAIN, HEX, SST, 1/4-32 /77250/ /334-0287-000/	1	

FIGURE AND. INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
14 - 60	AN936A4-16B	. WASHER /373-3050-000/.	1	
		---*---		
- 61	MS25036-145	. TERMINAL /304-1252-000/.	16	
- 62	MS25068-31	. SWITCH .266-0073-000/.	1	
- 63	69-4073	. SPEAKER /74199/ /271-0259-010/	1	
		-ATTACHING PARTS-		
	MS51959-30	. SCREW /342-0064-000/	4	
	68-NM62	. NUT, SLFLKG, HEX, AL, 6-32 /72962/ /333-0368-000/.	4	
		---*---		
- 64	793-6041-001	. GRILL SPEAKER.	1	
- 65	MS90311-231	. SWITCH /266-5192-000/.	2	
- 66	MS91528-2018	. KNOB /281-0122-000/ EFF TO REV LTR AN/	1	
	633-4570-002	. KNOB /EFF WITH REV LTR AN/	1	
- 67	383-0056-040	. ATTENUATOR, VAR /01121/ /383-0056-040/	1	
		-ATTACHING PARTS-		
	P313-0064-000	. NUT, PLAIN, HEX, SST, 3/8-32 /77250/ /313-0064-000/ /EFF TO REV LTR AF/	1	
	P313-0064-000	. NUT, PLAIN, HEX, SST, 3/8-32 /77250/ /313-0064-000/ REV LTR AF/	2	
	P313-0064-000	. NUT, PLAIN, HEX, SST, 3/8-32 /77250/ /313-0064-000/ EFF WITH REV LTR AL/	1	
	1720-02	. WASHER, LOCK, SST, 0.319 ID X 0.507 OD /78189/. . . /373-0085-000/ /EFF TO REV LTR AF/	1	
	1720-02	DELETED /EFF TO REV LTR AL/	1	
	AN960C616	. WASHER, FLAT, SST, 0.390 ID X 0.625 OD /81350/. . . 310-9001-020 /EFF WITH REV LTR AL/	1	
		---*--		
	AN960-10	. WASHER, LFAT, CS, 0.203 ID X 0.438 OD /88044/ . . . 310-9001-020 /EFF WITH REV LTR AL/	1	
		---*---		
- 68	MS41-12-1	. JACK /358-0014-000/	1	
- 68A	NAS1525M6H	. WASHER, FLAT TEFLON 3/8 IN..	1	
- 69	MS3112E10-65	. CONNECTOR /371-8510-010/	1	
		-ATTACHING PARTS-		
	MS51957-4	. SCREW /343-0125-000/ /EFF TO REV LTR AF/.	4	
	MS51957-14	. SCREW /343-0134--000/ /EFF WITH REV LTR AF/	4	
	310-6320-000	. WASHER, FLAT, 0.092 ID X 0.218 OD /79807/ . . . . . /310-6320-000/	4	
	MS35338-134	. WASHER, /310-0275-000/.	4	
	MS35649-224	. NUT /313-0037-000/.	4	
		---*---		
- 70	M39019/01-225	. CIRCUIT BREAKER, 3.0-AMP CURRENT RATING /81541/ . . /260-4053-110/	1	

FIGURE AND INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
14 - 71	MS90310-231	. SWITCH /266-5363-000/	1	
- 71A	623-9008-001	. HOUSEMARK /EFF WITH REV LTR AF/	1	
- 72	789-7558-004	. PLATE, IDENTIFICATION /EFF TO REV LTR AF/	1	
- 72	633-7891-001	. PLATE, IDENTIFICATION /EFF WITH REV LTR AF/	1	
- 73	769-7171-001	. HOLDER, IDENTIFICATION /EFF TO REV LTR AF/	1	
- 73	632-5201-001	. HOLDER, IDENTIFICATION /EFF WITH REV LTR AF/	1	
		-ATTACHING PARTS-		
	MS51959-13	. SCREW /342-0044-000/	2	
		---*---		
- 74	MS51957-32	. SCREW /343-0174-000/	4	
- 75	759-4321-001	. O-RING	4	
- 76	793-6037-002	. PANEL, EDGELIGHT	1	
- 77	JT08P12-98S014	. CONNECTOR, PLUG /77820/ /371-9008-060/	2	
- 78	JT08P16-55S014	. CONNECTOR, PLUG /77820/ /371-9008-160/	2	
- 79	795-8766-001	. NAMEPLATE /EFF TO REV LTR AF/	1	
- 79	795-8766-000	. NAMEPLATE /EFF WITH REV LTR AF/	1	
		-ATTACHING PARTS-		
- 80	330-4025-020	. SCREW, TAPPING, SST, 2-56 X 3/16 /45722/ /330-4025-020/	2	
		---*---		
	793-6013-001	. CHASSIS, AUDIO CONTROL	1	
		PARTIAL BREAKDOWN FOLLOWS		
- 81	FPN6-32SCL	. . NUT, PRESS, CD PL STL, 6-32 /83324/ /334-1152-000/	8	
	793-6256-001	. . PANEL, WELDED	1	
		-ATTACHING PARTS-		
	MS51959-29	. . SCREW /342-0063-000/	2	
		---*---		
- 82	H539-2	. . . STANDOFF /83014/ /012-4958-010/	4	
- 83	FPN6-32SCL	. . . NUT, PRESS, CD PL STL, 6-32 /83324/ /334-1152-000/	6	
- 84	F632-1	. . . NUT, PL, CLINCH, STL, 6-32 /46384/ /334-1476-000/	3	
- 85	793-6249-001	. . . BUSHING, INDICATOR LIGHT	5	
- 86	793-6052-001	. . PANEL, AUDIO, FABRICATED	1	
- 87	793-5978-001	. . BRACKET, CENTER MOUNTING	1	
		-ATTACHING PARTS-		
	MS20426AD4-5	. . RIVET /305-1374-000/	5	
		---*---		
- 88	793-5982-001	. . BRACKET, RIGHT FRONT	1	
		-ATTACHING PARTS-		
	MS20426AD4-5	. . RIVET /305-1374-000/	5	
		---*---		
- 89	793-5967-001	. . STRIP, FASTENER	2	
		-ATTACHING PARTS		
	MS20470AD4-6	. . RIVET /305-1171-000/	10	
		---*---		
- 90	793-5967-001	. . STRIP, FASTENER	1	
		-ATTACHING PARTS-		
	MS20470AD4-9	. . RIVET /305-1174-000/	5	
		---*---		
- 91	793-5967-001	. . STRIP, FASTENER	1	
		-ATTACHING PARTS-		
	AD438S	. . RIVET /61957/ /305-1298-000/	5	
		---*---		
- 92	793-5968-001	. . SPACER	1	
		-ATTACHING PARTS-		
	MS20426AD4-6	. . RIVET /305-1375-000/	2	
		---*---		
- 93	793-6012-003	. . BRACKET, FAB	1	
- 94	793-6012-00[illegible]	. . CHASSIS, FAB	1	

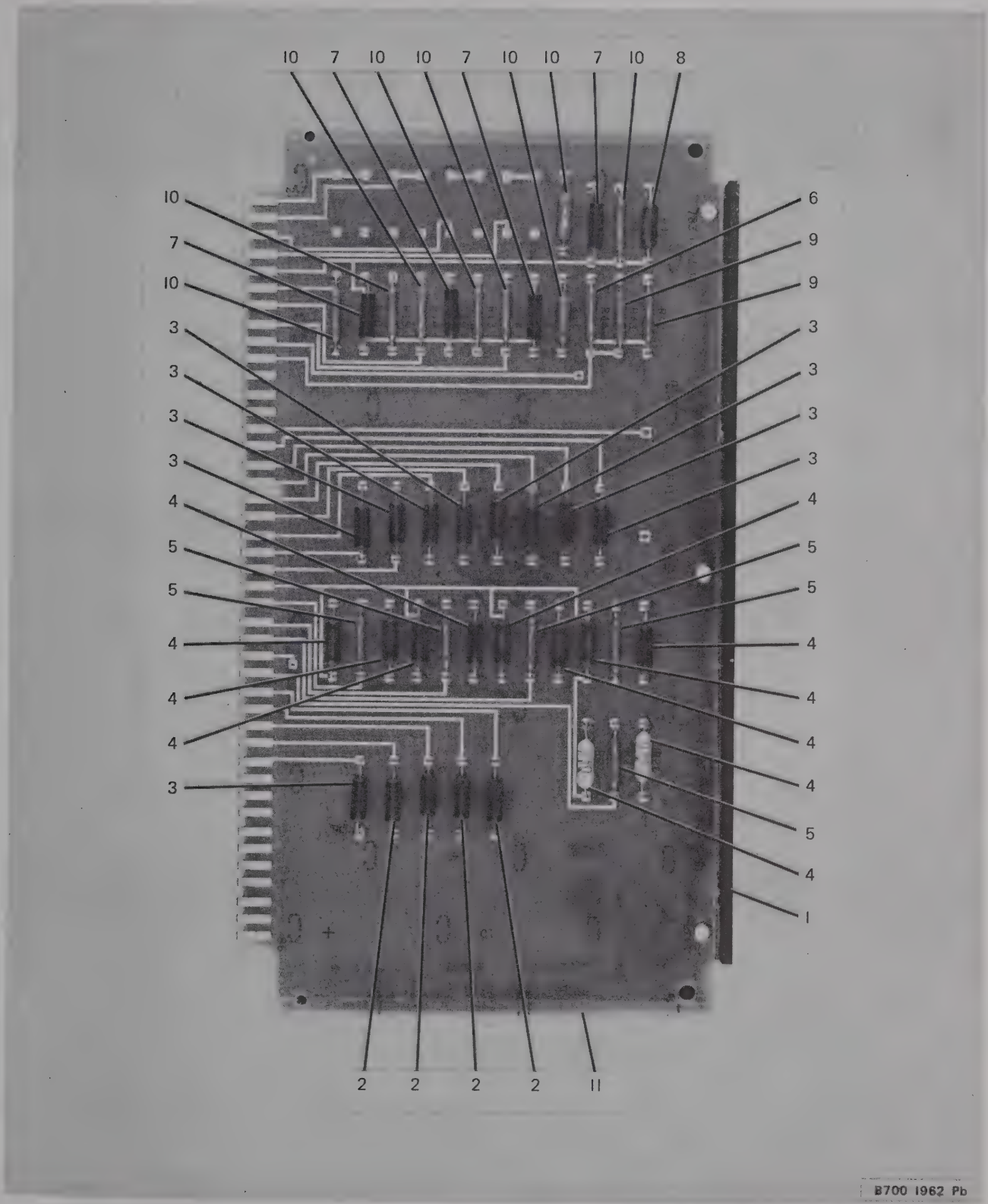

Figure 6-15. Audio Control Card A1

FIGURE AND INDEX NO.	PART NUMBER	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
15	783-1427-001	CARD, AUDIO CONTROL /SEE FIGURE 14 FOR NHA/	REF	
- 1	543-6358-003	. HANDLE.	1	
		-ATTACHING PARTS-		
	MS20470AD2-3	. RIVET /305-1141-000/	3	
		---•---		
- 2	RNC60H3010FR	. RESISTOR /724-1015-380/	4	
- 3	RNC60H5900FR	. RESISTOR /724-1015-520/	9	
- 4	RNC60H7150FR	. RESISTOR /724-1015-560/	10	
- 5	RNC60H9090FR	. RESISTOR /724-1015-610/	5	
- 6	RNC60H9530FR	. RESISTOR /724-1015-620/	1	
- 7	RNC60H3831FR	. RESISTOR /724-1015-910/	4	
- 8	RNC60H4421FR	. RESISTOR /724-1015-940/	1	
- 9	RNC60H5111FR	. RESISTOR /724-1015-970/	2	
- 10	RNC60H5901FR	. RESISTOR /724-1016-010/	8	
- 11	600-9077-012	. BOARD	1	

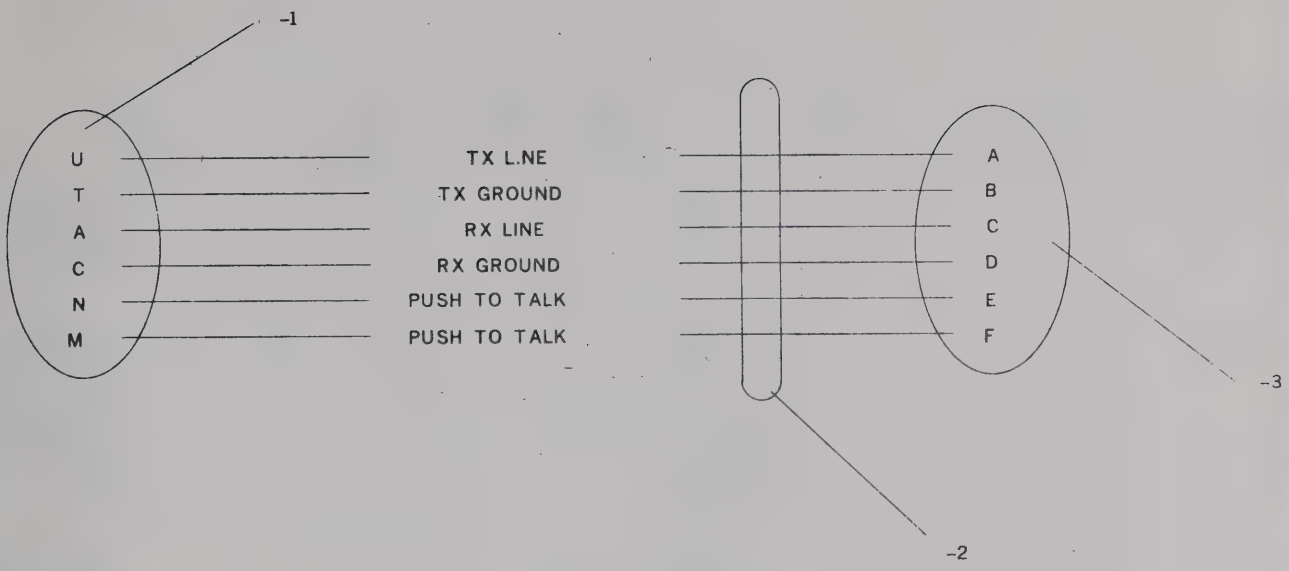

Figure 6-16. KY-65 Interconnect Cable

Figure and Index No.	Part Number	Description 1 2 3 4 5 6 7	Units Per Assy	Usable on Code
16-		KY-16 Interconnect Cable		
16-1	MS3116F16-26S	. Connector, KY-65	1	PAFZZN
16-2	0910001A	. Cable, 10 ft	1	PAFZZN
16-3	MS3476L10-6P	. Connector, OK-145	1	PAFZZN

SECTION III
NUMERICAL INDEX

PART NUMBER	FIG. AND INDEX NO.	QTY. PER ART.	SOURCE CODE	REPAIR CODE
A043BS	14 - 91	5		
AM25S80DMB0037	4A- 10	1		
AM27S80DMB0036	4A- 9	1		
AN936A416B	14 - 60	1	P1	S
AN960-10	14 - 67	1		
AN960C516	14 - 67	1		
	14 - 70	1	P1	S
A086312	14 - 50	1	P1	S
A7K37051422A	8 - 18	4		
CKR05BK104MM	4A- 2	12		
CK05BX222K	8 - 12A	1		
CK05BX470K	11 - 25	2	P1	S
CK07BX181K	7 - 18	2	P1	S
CK07BX221K	3 - 30	2	P1	S
CK07BX470K	6 - 33	1	P1	S
CK07BX561K	6 - 34	2	P1	S
	8 - 41			
CK31BT102K	5 - 17	13	P1	S
	9 - 14			
CK31BT102M	9 - 14	12		
CK31BT392K	8 - 42	1	P1	S
CK31BV513K	6 - 35	1	P1	S
CK32BV104M	3 - 31	29	P1	S
	4 - 29			
	5 - 18			
	6 - 36			
	7 - 19			
	8 - 43			
	9 - 15			
CK63AW103M	2 - 52D	4	P1	S
	12 - 6			
CK63CZ332M	12 - 3	1	P1	S
CL832-2C	10 - 14	4	P1	S
CM05FD391GP3	12 - 3A	4		
CP09A1KC224K3	14 - 38A	1	P1	S
C22A223K	11 - 16	1	P1	S
DIE845	2 - 14	18		
	2 - 17			
	F2 - 25			
	F2 - 55			
	13 - 11			
	13 - 14			
	13 - 21			
	13 - 52			
FPN4-40SCL	10 - 3	4	P1	S
FPN6-32SCL	14 - 20	40	P1	S
	14 - 22			
	14 - 25			
	14 - 27			
	14 - 29			
	14 - 31			
	14 - 33			
	14 - 39			
	14 - 43			
	14 - 45			
	14 - 81			
	14 - 83			
F51K2	4 - 1	5	P1	S
	5 - 2			
	6 - 5			

PART NUMBER	FIG. AND INDEX NO.	QTY. PER ART.	SOURCE CODE	REPAIR CODE
F632-1	14 - 84	3	P1	S
G140K2	6 - 2	1	P1	S
G191K2	5 - 1	2	P1	S
	6 - 4			
G371K2	4 - 15	9	P1	S
	6 - 13			
	7 - 13			
	8 - 20			
G380K2	8 - 19	1	P1	S
G5448X152M	3 - 29	3	P1	S
	6 - 31			
	8 - 41			
G5448X181M	7 - 18	2		
G5448X182J	4 - 28	2	P1	S
	6 - 32			
G5448X470J	6 - 33	1		
G5448X561J	6 - 34	1		
HL11554	5 - 10	2	P1	S
	7 - 11			
HL11561	4 - 7	10	P1	S
	8 - 14			
HL30110	4 - 16	2	P1	S
HP10N	14 - 6	2	P1	S
HP4N	14 - 7	1	P1	S
HP5N	14 - 7	1		
HP6N	14 - 8	2		
	14 - 8A			
HP7N	14 - 8	2	P1	S
	14 - 9			
HP8N	2 - 33	5	P1	S
	13 - 28			
	14 - 7A			
	14 - 9			
H08014S	4 - 11	1	P1	S
H08015S	4 - 12	1	P1	S
H10004S	4 - 9	1	P1	S
H10005S	4 - 10	1	P1	S
H12014S	4 - 13	1	P1	S
H12015S	4 - 14	1	P1	S
H538-30-10	14 - 53	4	P1	S
H539-2	14 - 82	4	P1	S
JAN1N4500	11 - 23	8		
JTG06A14-37P014	2 - 22	2	P1	S
	13 - 19			
JTP02RE12-98P014	2 - 38	2	P1	S
	13 - 33			
JTP02RE14-37S014	2 - 43	2	P1	S
	13 - 38			
JTP02RE16-55P014	2 - 30	2	P1	S
	13 - 25			
JT08P12-98S014	14 - 77	2	P1	S
JT08P16-55S014	14 - 78	2	P1	S
JW33-1114A	14 - 10	3	P1	S
LHTA51M2860-62	2 -101	4	P1	S
	13 - 94			
LHTA57M2860-40	2 - 57A	15	P1	S
	2 - 58A			
	2 - 58E			
	13 - 55			
	13 - 55C			

PART NUMBER	FIG. AND INDEX NO.	QTY PER ART.	SOURCE CODE	REPAIR CODE
MRPN6-32SCL	2-103	8	P1	S
	13- 96			
MS20425AD2-3	2-	120	P1	S
	2-			
	2-			
	2-			
	2-102			
	13-			
	13-			
	13-			
	13-			
	13- 95			
MS20426AD2-4	2- 57	45	P1	S
	2- 58			
	2- 58D			
	13-			
	13-			
MS20425AD4-5	14-	10		
	14-			
MS20425AD4-6	14-	2		
MS20470AD2-3	15-	3	P1	S
MS2-470AD2-6	14-	10	P1	S
MS20470D4-9	14-	5	P1	S
MS24515-685	14- 54	26	P1	S
	6- 2-61			
	6- 2-67			
	6-13-58			
	6-13-64			
MS24630-2	13-	REF		
MS24693C24	2- 26	8	P1	S
	13- 22			
MS24693C25	2- 3	52	P1	S
	2- 28			
	2- 57			
	13- 3			
	13- 24			
	13- 54			
MS25036-145	14- 61	16	P1	S
MS25063-31	14- 62	1	P1	S
MS27183-3	10-	9	P1	S
	10-			
	10-			
	10-			
MS3102R10SL3P	14- 5	1	P1	S
MS3112E10-65	14- 69	1	P1	S
MS3112E22-55P	14- 4	1	P1	S
MS3116F16-26S	16-1	1	PAFZZN	
MS3367-4-9	2- 52C	400		
	2- 99D			
	13- 48B			
	13- 75C			
MS3476L10-6P	16-3	1	PAFZZN	
MS35333-72	2-	8	P1	S
	2- 50			
	13-			
	13- 45			
MS35338-134	14-	14	P1	S
	14-			
	14-			
	14-			
MS35338-135	12-	6	P1	S
	14-			
MS35338-136	12-	32	P1	S
	14-			
	14-			
	14-			
	14-			
	14-			
	14-			
	14-			
	14-			
	14-			
	14-			
	14-			
MS35489-4	14-5F	1	P1	S
MS35649-224	2-72	28	P1	S
	10-			
	13-			
	13-69			
	14-			
	14-			
	14-			
	14-			
MS35649-244	2-42	2	P1	S
	13-37			
MS35650-304	14-	4	P1	S
MS51957-13	10-	9	P1	S
	10-			
	10-			
	10-			
MS51957-14	2-	16	P1	S
	2-13			
	2-34			
	13-			
	13-10			
	13-29			
MS51957-14	14-		P1	S
MS51957-15	2-	26	P1	S
	2-31			
	2-39			
	2-44			
	13-26			
	13-34			
	13-39			
MS51957-16	2-41	2	P1	S
	13-36			
MS51957-17	14-	2	P1	S
MS51957-18	2-16	4	P1	S
	13-13			

PART NUMBER	FIG. AND INDEX NO.	QTY PER ART.	SOURCE CODE	REPAIR CODE
MS51957-21	2-	4	P1	S
	13-			
MS51957-24	14- 2	3	P1	S
MS51957-26	14-	3		
MS51957-28	14-	23	P1	S
	14-			
	14-			
	14-			
	14-			
	14-			
	14- 3			
MS51957-29	14-	4	P1	S
	14-			
MS51957-3	12-10	2	P1	S
	12-11			
MS51957-30	14-	4		
MS51957-308	14-	1		
	14-			
MS51957-31	14-	4	P1	S
MS51957-32	14-74	4	P1	S
MS51957-4	2-19	22	P1	S
	13-16			
	14-			
	14-			
	14-			
	14-			
MS51957-42	2-48	6	P1	S
	13-46			
MS51957-43	2-49	2	P1	S
	13-44			
MS51957-9	2-	8	P1	S
	2-			
	13-			
	13-			
MS519578-63	14-41	6	P1	S
	14-49			
MS51959-1	2-	5	P1	S
	13-			
MS51959-12	10-	3	P1	S
MS51959-13	14-	2	P1	S
MS51959-14	2-97	26	P1	S
	2-99			
	10-			
	13-90			
	13-92			
MS51959-17	10-	3	P1	
	10-			
MS51959-2	2-	5		

PART NUMBER	FIG.AND INDEX NO.	QTY PER ART.	SOURCE CODE	REPAIR CODE
	13-	2	P1	S
MS51959-27	10-	8	P1	S
MS51959-28	14-			
	14-			
	14-			
	14-	25	P1	S
MS51959-29	14-			
	14-			
	14-			
	14-			
	14-			
	14-			
	14-			
	14-			
	14-42	8	P1	S
MS51959-3	2-69			
	13-66	4	P1	S
MS51959-30	14-	14	P1	S
MS51959-4	2-69			
	10-			
	13-			
	13-66	2	P1	S
MS51960-64	14-48	8	P1	S
MS51963-9	14-	1	P1	S
MS75028-23	2-29	1	P1	S
MS90310-231	14-71	1	P1	S
MS90311-211	2-89	2	P1	S
MS90311-30	14-65	2	P1	S
	11-20			

PART NUMBER	FIG. AND INDEX NO.	QTY. PER ART	SOURCE CODE	REPAIR CODE
MS90537-41	11 - 19	1	P1	S
MS90537-45	6 - 1	1	P1	S
MS91189-30	12 - 12	2	P1	S
MS91528-0D1B	2 - 60	3		
	13 - 57			
	14 - 59			
MS91528-0H1B	2 - 59	19	P1	S
	13 - 56			
	14 - 57			
MS91528-1D2B	14 - 66	1	P1	S
M21097-1-136	9 - 11	1	P1	S
M21097-8-4	14 - 36	1	P1	S
M21097-9-01	14 - 34A	172	P1	S
M22-01-00091SB	2 - 91	2	P1	S
	13 - 84			
M38510-02002BCB	4A- 18	1		
M38510-02004BCB	4A- 7	1		
M39003-01-2005	11 - 6	1	P1	S
M39003-01-2026	12 - 8	4	P1	S
M39003-01-2047	11 - 27	1	P1	A
M39003-01-2062	11 - 21	2	P1	S
M39003-01-2117	3 - 32	1	P1	S
M39003-01-2140	11 - 22	4	P1	S
M39003-01-2255	8 - 1	1	P1	S
M39003-01-2271	3 - 33	5	P1	S
	6 - 37			
	8 - 2			
M39003-01-2272	9 - 1	1	P1	S
M39003-01-2296	4A- 17	1		
M39003-01-2331	8 - 3	1	P1	S
M39018-01-0674	12 - 18	5	P1	S
M39019-01-225				
M39024-11-03	9 - 8	1	P1	S
M39024-11-04	9 - 9	1	P1	S
M641-12-1	14 - 68	1	P1	S
NAS1068A06	2 - 4	54	P1	S
	2 - 54			
	2 -100			
	13 - 4			
	13 - 51			
	13 - 93			
NAS1515M6H	14 - 68A	1		
NAS697C06	13 - 94	REF		
NCN4-1-3	10 - 13	2	P1	S
PFSC3 1-2 38	2 -105	20	P1	S
	13 - 98			
PM23-3-0-750A	14 - 47	1	P1	S
P313-0045-000	2 - 27	32	P1	S
	13 - 23			
	14 - 6			
	14 - 7			
	14 - 7			
	14 - 8			
	14 - 9			
	14 - 17			
	14 - 38			
	14 - 5A			
	14 - 5D			
	14 - 8A			

PART NUMBER	FIG. AND INDEX NO.	QTY. PER ART	SOURCE CODE	REPAIR CODE
P313-0064-000	14 - 67	4	P1	S
	14 - 67			
	14 - 67			
P313-0132-000	14 - 36	2	P1	S
P313-0140-000	12 - 15	4	P1	S
P313-0156-000	12 - 15	4		
P334-0287-00	2 - 74	17	P1	S
	2 - 79			
	2 - 82			
	2 - 85			
	2 - 92			
	13 - 71			
	13 - 74			
	13 - 77			
	13 - 85			
P334-2087-000	14 - 60	1		
P343-0035-000	2 - 64	12	P1	S
	13 - 61			
P343-0290-000	12 - 15	4		
P343-0333-000	12 - 15	4	P1	S
P347-0032-000	14 - 17	3	P1	S
RCR05G102JS	4A- 12	2	P1	S
	6 - 21			
	8 - 38			
RCR05G102K	3 - 24	4	P1	S
	6 - 27			
RCR05G102KS	4A- 3	5		
RCR05G103JS	3 - 23	10	P1	S
	8 - 32			
	8 - 38			
	9 - 12			
RCR05G103K	3 - 28	23	P1	S
RCR05G103K	6 - 30			
	8 - 31			
	8 - 36			
RCR05G103KS	4A- 11	8		
RCR05G104JS	9 - 13	24	P1	S
RCR05G123JS	8 - 38	AR	P1	S
RCR05G151K	6 - 26	1	P1	S
RCR05G152JS	8 - 38	AR	P1	S
RCR05G153JS	8 - 38	AR	P1	S
RCR05G183JS	8 - 38	AR	P1	S
RCR05G222JS	8 - 38	AR	P1	S
RCR05G222K	3 - 25	4	P1	S
RCR05G223JS	4A- 14	1	P1	S
	8 - 38			
RCR05G223K	8 - 37	15	P1	S
RCR05G272JS	3 - 19	1	P1	S
RCR05G272K	8 - 34	5	P1	S
RCR05G273JS	8 - 38	AR	P1	S
RCR05G331K	5 - 14	1	P1	S
RCR05G332JS	3 - 20	2	P1	S
	6 - 22			
	8 - 38			
RCR05G333JS	6 - 25	1	P1	S
	8 - 38			
RCR05G392JS	8 - 38	AR	P1	S
RCR05G432JS	3 - 21	3	P1	S
	6 - 23			

PART NUMBER	FIG. AND INDEX NO.	QTY. PER ART	SOURCE CODE	REPAIR CODE
RCR05G471JS	8 - 29	3	P1	S
RCR05G471K	5 - 15	3	P1	S
RCR05G472JS	8 - 38	AR	P1	S
RCR05G472K	3 - 26	14	P1	S
	4 - 27			
	6 - 28			
	8 - 35			
RCR05G512JS	F3 - 21	1		
RCR05G561JS	8 - 30	2	P1	S
RCR05G562JS	6 - 24	1	P1	S
	8 - 38			
RCR05G680K	8 - 33	1	P1	S
RCR05G681JS	8 - 38	AR	P1	S
RCR05G682JS	3 - 22	3	P1	S
	8 - 31			
	8 - 38			
RCR05G682K	6 - 17	1	P1	S
RCR05G821K	5 - 16	2	P1	S
RCR05G822JS	8 - 38	AR	P1	S
RCR05G822K	3 - 27	2	P1	S
	6 - 29			
RCR05G910JS	8 - 28	1	P1	S
RCR07G100KS	3 - 18	2	P1	S
RCR07G102KS	12 - 20	2	P1	S
RCR07G103KS	11 - 7	3	P1	S
RCR07G220KS	11 - 15	2	P1	S
RCR07G221KS	11 - 13	2	P1	S
RCR07G362JS	6 - 22	1		
RCR07G392JS	6 - 23	2		
RCR07G682KS	11 - 26	1	P1	S
RCR07G820KS	11 - 14	1	P1	S.

PART NUMBER	FIG. AND INDEX NO.	QTY. PER ART	SOURCE CODE	REPAIR CODE
RE65G10R0	13 - 42	2	P1	S
RH5X000B10001F	10 - 9A	1		
RNC60H1000FR	11 - 8	2	P1	S
RNC60H1101FR	11 - 9	1		
RNC60H3010FR	15 - 2	4	P1	S
RNC60H3831FR	15 - 7	4	P1	S
RNC60H4421FR	15 - 8	1	P1	S
RNC60H5110FR	11 - 11	3	P1	S
RNC60H5111FR	15 - 9	2	P1	S
RNC60H5620FR	11 - 12	1	P1	S
RNC60H5900FR	15 - 3	9	P1	S
RNC60H5901FR	15 - 10	8	P1	S
RNC60H7150FR	15 - 4	10	P1	S
RNC60H7500FR	11 - 10	2	P1	S
RNC60H9090FR	15 - 5	5	P1	S
RNC60H9530FR	15 - 6	1	P1	S
RNR55J1002FM	4 - 25	2	P1	S
RNR55J2492FM	4 - 26	1	P1	S
RNR55J2611FM	4 - 30	1	P1	S
RNR55J2742FM	8 - 39	AR	P1	S
RNR55J2802FM	8 - 39	AR	P1	S
RNR55J2872FM	8 - 39	AR	P1	S
RNR55J2942FM	8 - 39	AR	P1	S
RNR55J3012FM	8 - 39	AR	P1	S
RNR55J3092FM	8 - 39	AR	P1	S
RNR55J3162FM	8 - 39	AR	P1	S
RNR55J3242FM	8 - 39	AR	P1	S
RNR55J3322FM	8 - 39	AR	P1	S
RNR55J6492FM	8 - 40	AR	P1	S
RNR55J6652FM	8 - 40	AR	P1	S
RNR55J6812FM	8 - 40	AR	P1	S
RNR55J6982FM	8 - 40	AR	P1	S

PART NUMBER	FIG. AND INDEX NO.	QTY. PER ART	SOURCE CODE	REPAIR CODE
RNR55J7152FM	8 - 40	AR	P1	S
RNR55J7322FM	8 - 40	AR	P1	S
RNR55J7502FM	8 - 40	AR	P1	S
RNR55J7682FM	8 - 40	AR	P1	S
RNR55J7872FM	8 - 40	AR	P1	S
RN60D1961F	11 - 10A	1	P1	S
RT22C2P101	11 - 5	2	P1	S
RW69V1R8	12 - 17	1	P1	S
RW69V101	13 - 41	1	P1	S
RW69V151	12 - 2	1	P1	S
RW69V2R7	12 - 1	2	P1	S
SD7726A	8 - 11	2	P1	S
SD7727A	7 - 8	5	P1	S
SD9857A	3 - 5	11	P1	S
	4 - 5			
	9 - 6			
SF10112	5 - 3	9	P1	S
	6 - 6			
SG14127	6 - 3	5	P1	S
	7 - 2			
	8 - 7			
	9 - 2			
SG8025	6 - 7	1	P1	S
SG812	7 - 3	1	P1	S
SM2014	7 - 5	1	P1	S
SM7037A	8 - 13	8	P1	S
SNC54LS161J	4A- 1	3		
SNC54LS251J	4A- 15	1		
SNC54LS76J	4A- 5	3		
SNC54LS91J	4A- 8	2		
SN19670	4 - 6	2		
SSTINAT	2 - 52C	400		
	2 - 99D			
	13 - 49B			
	13 - 75C			
SS314	4 - 2	7	P1	S
	7 - 4			
TF300	2 - 53	5	P1	S
	13 - 49			
TLC213MOD	14 - 14	1	P1	S
TLC333C	14 - 11	2	P1	S
TLC333C1	14 - 11	2		
TLC407MOD	14 - 13	1	P1	S
TLC501MOD	14 - 12	1	P1	S
UD4225	3 - 6	3	P1	S
W1048	2 - 87	2	P1	S
	13 - 82			
W1044CE	2 - 87	2		
	13 - 82			
0910001A	16 - 2	1	FAFZZN	
1N647	10 - 8A	1	P1	S
10-352421-14	2 - 23	2	P1	S
	13 - 20			
100-200-9-23	14 - 38B	1	P1	S
1214-05COPL	2 - 75	17	P1	S
	2 - 80			
	2 - 83			
	2 - 86			
	2 - 93			
	13 - 72			
	13 - 75			
	13 - 78			
	13 - 86			
12397-93015L	5 - 9	1	P1	S
12483	8 - 15	1	P1	S
130GOLD	2 - 90	2	P1	S
	13 - 81			
160A604GRN	2 - 76A	8	P1	S
	13 - 79A			
	14 - 55A			
160A604RED	2 - 77A	2	P1	S
	13 - 78A			
160A604WHT	14 - 54A	4	P1	S
1720-02	14 - 67	1	P1	S
	14 - 67			
183-0101-1474-60	2 - 66	2	P1	S
	13 - 63			
183-1474-001	2 - 62A	2	P1	S
	13 - 59A			
2104-06-02-2520N	14 - 17	8	P1	S
2104-08-02-2520N	2 - 51	2	P1	S
	13 - 47			
2115	12 - 38	2		
259-2641-020	14 - 58	4	P1	S
259-2769-010	2 - 73	5	P1	S
	13 - 76			
259-2769-020	13 - 73	2	P1	S
259-2769-030	2 - 78	1	P1	S
259-2769-050	2 - 94	1	P1	S
259-2769-060	13 - 70	5	P1	S
259-2769-090	2 - 81	1	P1	S

PART NUMBER	FIG. AND INDEX NO.	QTY PER ART	SOURCE CODE	REPAIR CODE
280-1339-010	2 - 2	2		
	13 - 2			
280-1339-130	10 - 2	1		
280-3035-000	2 - 2	2	U	S
	13 - 2			
3-18536	12 - 13	1	P1	S
3-18572	10 - 9	1	P1	S
302-4800-000	2 - 55	10	P1	S
	10 - 10			
	13 - 52			
302-7000-000	12 - 10	1	P1	S
310-0046-000	14 - 6	25	P1	S
	14 - 7			
	14 - 7			
	14 - 8			
	14 - 9			
	14 - 17			
	14 - 18			
	14 - 5A			
	14 - 5D			
	14 - 8A			
310-0049-000	14 - 41	8	P1	S
	14 - 44			
310-0054-000	12 - 15	8	P1	S
310-0055-000	12 - 15	8	P1	S
310-0070-000	2 - 21	22	P1	S
	2 - 71			
	10 - 9A			
	13 - 18			
	13 - 42			
	13 - 68			
310-0073-000	14 - 41	8	P1	S
	14 - 44			
310-0081-000	12 - 4	5	P1	S
	12 - 5			
310-0131-000	12 - 15	8		
310-0277-000	10 - 1	9	P1	S
	10 - 5			
	10 - 7			
	10 - 10			
310-0278-000	2 - 15	8	P1	S
	2 - 18			
	2 - 36			
	13 - 12			
	13 - 15			
	13 - 31			
310-6320-000	2 - 20	40	P1	S
	2 - 70			
	2 - 94			
	2 - 95			
	12 - 10			
	12 - 11			
	13 - 17			
	13 - 67			
	13 - 87			
	13 - 88			
	14 - 4			
	14 - 5			
	14 - 38			
	14 - 69			
310-6340-000	2 - 35	6	P1	S
	13 - 30			
	14 - 36			
317-187	8 - 27	3	P1	S
318-0035	2 - 88	2	P1	S
	13 - 83			
330-4025-020	1 - 1	8	P1	S
	2 - 1			
	13 - 1			
	14 - 80			
334-1008-000	12 - 4	5	P1	S
	12 - 5			
3340	14 - 17A	3	P1	S
351-0024-010	8 - 4	1	P1	S
351-0025-010	8 - 5	1	P1	S
351-1523-032	4A- 16	2		
351-1605-011	4A- 4	4		
351-2022-010	8 - 6	1	P1	S
351-7436-012	4 - 8	6	P1	S
	6 - 12			
	8 - 16			
351-7437-012	3 - 7	2	P1	S
	7 - 12			
351-7445-012	3 - 8	3	P1	S
	8 - 17			
352-0551-041	6 - 16	1	P1	S
352-0661-041	6 - 15	3	P1	S
352-7500-191	3 - 9	7	P1	S
	11 - 2			
352-7500-281	3 - 10	7	P1	S

PART NUMBER	FIG. AND INDEX NO.	QTY. PER ART.	SOURCE CODE	REPAIR CODE
352-7500-281	4 - 18			
	11 - 1			
352-7500-491	12 - 15	2	P1	S
352-7500-781	6 - 16	1	P1	S
353-2710-001	6 - 17	1		
353-2850-001	4A- 13	1		
353-2852-001	10 - 8A	1	P1	S
353-2906-001	6 - 18	1	P1	S
353-2978-001	3 - 12	4	P1	S
	4 - 19			
	6 - 17			
353-3129-001	8 - 22	1		
353-3337-001	11 - 23	8	P1	S
353-3338-001	3 - 13	4	P1	S
	4 - 20			
	6 - 18			
353-3625-011	11 - 4	2	P1	S
353-3656-031	9 - 7	70	P1	S
353-6080-001	12 - 5	1	P1	S
353-6522-041	8 - 21	1		
353-9008-011	11 - 3	5	P1	S
353-9009-011	12 - 4	4	P1	S
353-9009-061	12 - 16	4	P1	S
353-9010-201	8 - 22	1	P1	S
353-9010-261	8 - 21	1	P1	S
37T88	14 - 38	1	P1	S
3705DMQB	8 - 18	4		
372-2234-010	3 - 16	246	P1	S
	4 - 23			
	5 - 13			
	6 - 20			
	7 - 16			
	8 - 25			
372-2234-020	3 - 17	138	P1	S
	4 - 24			
	7 - 17			
	8 - 26			
372-2235-010	12 - 22	2		
	12 - 24			
372-2236-010	12 - 20A	14		
372-2252-010	11 - 16A	15	P1	S
372-2255-010	2 - 52A	31	P1	S
	2 - 99C			
	13 - 48			
	13 - 75A			
372-2255-020	2 - 52B	233	P1	S
	2 - 99B			
	13 - 6			
	13 - 48A			
	13 - 75B			
372-2601-045	2 - 56A	373	P1	S
	13 - 53A			
372-2601-057	9 - 10	76	P1	S
372-2602-012	12 - 21	7		
	12 - 23			
372-2602-013	12 - 21	6		
	12 - 23			
372-2621-013	4 - 21	3	X2	S
	4A- 6			
	8 - 23			
372-2621-014	5 - 11	2	X2	S
	7 - 14			
372-2621-015	6 - 19A	1	X2	S
372-2621-021	3 - 15	1	X2	S
372-2621-045	5 - 12	2	X2	S
	6 - 19			
372-2623-045	3 - 14	5	P1	S
	4 - 22			
	4A- 19			
	7 - 15			
	8 - 24			
372-2624-011	11 - 17	1	P1	S
372-2625-017	11 - 18	1	P1	S
372-2626-045	2 - 46	1	P1	S
	13 - 7			
372-2626-047	13 - 50	1		
381	2 - 62	2	P1	S
	13 - 59			
383-0056-040	14 - 67	1	P1	S
4JX14	14 - 16	2	P1	S
41C92	12 - 7	4	P1	S
41170	14 - 37	31	P1	S
	2 - 67			
	13 - 58			
	13 - 64			
456-01-25-788	14 - 35	1	P1	S
5160-458-604GRN	2 - 76	8	P1	S
	13 - 80			
	14 - 56			

PART NUMBER	FIG. AND INDEX NO.	QTY. PER ART.	SOURCE CODE	REPAIR CODE
5160-458-604RED	2 - 77	2	P1	S
	13 - 79			
5160-458-604WHT	14 - 55	4	P1	S
54L00SD7722A	3 - 1	51	P1	S
	4 - 3			
	5 - 4			
	6 - 8			
	7 - 6			
	8 - 8			
	9 - 3			
54L10SD7723A	3 - 2	16	P1	S
	5 - 5			
	6 - 9			
	7 - 7			
	8 - 9			
54L20SD7724A	3 - 3	10	P1	S
	4 - 4			
	5 - 6			
	6 - 10			
	8 - 10			
	9 - 4			
54L30SD7725A	5 - 7	2	P1	S
	9 - 5			
54L72SD7730A	6 - 11	2	P1	S
	7 - 9			
54L73SD8545A	3 - 4	10	P1	S
	5 - 8			
	7 - 10			
	8 - 12			
54L73SN14834	8 - 12	2		
540-9033-003	10 - 11	2	P1	S
540-9054-003	10 - 6	4	P1	S
	10 - 10			
540-9176-003	2 - 37	2	P1	S
	13 - 32			
540-9225-003	14 - 18	2	P1	S
541-5979-002	10 - 8	1	P1	S
543-6358-003	15 - 1	1	X2	S
5602-10-62	12 - 10	1		
5602-58-16	12 - 11	1	P1	S
5610-59-32	2 - 65	6		
600-0044-007	3 - 34	1		
600-0133-011	11 - 28	1		
600-0133-012	12 - 25	1		
600-3990-401	4A- 20	1		
600-9276-011	2 - 56B	1		
	13 - 53B			
600-9283-011	9 - 16	1		
600-9283-012	4 - 31	1		
600-9283-013	6 - 38	1		
600-9284-007	5 - 19	1		
600-9286-010	7 - 20	1		
600-9364-010	8 - 44	1		
607-2418-001	13 - 5	1	M	S
607-7702-001	12 - 22	3		
607-7703-001	12 - 20	1		
607-7710-001	12 - 19	1	P1	S
610-1501-001	10 - 12	1	X2	S
610-1524-001	10 - 1	1	P1	S
616-7289-001	14 - 5C	2	P1	S
616-7290-001	14 - 5E	1	P1	S
616-7291-001	14 - 5B	1	P1	S
616-7292-001	14 - 5A	1	X2	S
623-9008-001	14 - 71A	1		
624-9726-001	13 - 49	1		
632-5201-001	14 - 73	1		
633-4510-001	13 - 57	1		
633-4570-001	2 - 60	1		
633-4570-002	14 - 66	1		
633-7891-001	14 - 72	1		
633-9332-001	2 - 7	1		
	4A- 31			
68NM26	2 - 94	8	P1	S
	2 - 95			
	13 - 87			
	13 - 88			
68NM40	2 - 32	22	P1	S
	2 - 40			
	2 - 45			
	13 - 27			
	13 - 35			
	13 - 40			
68NM62	10 - 9	6	P1	S
	14 - 63			
69-4073	14 - 63	1	P1	S
7C36	2 - 68	2	P1	S
	13 - 65			
749-4728-050	14 - 60	1	P1	S
759-4321-001	2 - 65	16	P1	S
	13 - 62			

PART NUMBER	FIG. AND INDEX NO.	QTY. PER ART.	SOURCE CODE	REPAIR CODE
759-4321-001	14 - 75			
763-3339-003	14 - 52	2	X2	S
763-3340-001	14 - 51	4	P1	S
763-3341-001	14 - 50	4	P1	S
767-1421-001	4 - 17	58	X2	S
	6 - 14			
768-5919-003	2 - 56	6	P1	S
	13 - 53			
769-7171-001	14 - 73	1	X2	S
7717-130DAP	3 - 11	5	P1	S
7717-160AP	11 - 24	8	P1	S
775-4660-007	2 - 58B	24	M1	S
	2 - 58			
	13 - 55A			
	13 - 55D			
78S11M1005	14 - 15	5	P1	S
783-1427-001	14 - 19	1	P1	F
	15 - 94			
787-6444-001	1 - 3	1	P1	D
	13 - 25			
787-6487-001	1 - 2	1	P1	D
	2 - 4			
789-2583-005	13 - 60	1	M1	S
789-2584-005	2 - 63	1	X2	S
789-2587-001	13 - 92	1	A1	S
789-2588-002	13 - 52	1	X2	S
789-2588-003	2 - 55	1	X2	S
789-2589-001	2 - 99	1	X2	S
789-2590-001	2 - 96	8	M	S
	13 - 89			
789-2591-001	13 - 62	1	A1	S
789-2592-001	2 - 56	2	A1	S
	13 - 53			
789-2593-001	13 - 21	1	A1	S
789-2594-001	2 - 65	1	A1	S
789-2596-001	2 - 25	1	A1	S
789-2597-001	2 - 58G	2	X1	S
	13 - 55E			
789-2612-001	2 - 12	2	P1	D
	9 - 44			
	13 - 9			
789-2618-001	2 - 8	1	P1	D
	5 - 20			
789-2620-001	2 - 7	1	P1	D
	4 - 34			
789-2622-001	2 - 9	1	P1	D
	6 - 19			
789-2624-001	2 - 10	1	P1	D
	7 - 38			
789-2626-001	2 - 55	2	P1	D
	13 - 52			
789-2636-001	2 - 58	2	M1	S
	13 - 55			
789-2637-001	2 - 98	6	M	S
	13 - 91			
789-2639-002	2 - 5	2	X1	S
	13 - 5			
789-2640-001	2 - 2	1	M	S
789-2640-002	13 - 2	1	M	S
789-2641-001	2 - 58J	2	X2	S
	13 - 55G			
789-2652-001	2 - 94	2	X1	S
	13 - 88			
789-2653-001	2 - 95	2	X1	S
	13 - 87			
789-2656-001	2 - 58C	2	X1	S
	13 - 55B			
789-2657-001	2 - 57	2	M1	S
	13 - 54			
789-2658-001	13 - 50	1	X2	S
789-2660-001	2 - 53	1	X2	S
789-2666-001	2 - 25	4	P1	S
	13 - 21			
789-2667-001	2 - 24	2	X1	S
	13 - 20A			
789-2679-001	13 - 99	1	X2	S
789-2680-001	2 -106	1	X2	S
789-7497-001	1 -	1	A1	D
789-7558-004	14 - 72	1	X2	S
789-8117-001	1 - 4	1	A1	D
	14 - 99			
793-3374-001	12 - 14	1	X2	S
793-3378-001	10 - 1	1	X2	S
793-3378-002	10 - 4	1	X2	S
793-5949-002	14 - 46	1		
793-5950-001	14 - 44	1	X2	S
793-5956-002	14 - 34	1	X2	S
793-5957-002	14 - 44	1	X2	S
793-5958-001	14 - 40	1	X2	S
793-5960-002	14 - 21	1	X2	S
793-5961-001	14 - 19	1	X2	S
793-5964-001	14 - 32	2	X2	S
793-5967-001	14 - 89	4	X2	S
	14 - 90			
	14 - 91			
793-5968-001	14 - 92	1	X2	S
793-5978-001	14 - 87	1	X2	S
793-5980-002	14 - 26	1	X2	S
793-5981-001	14 - 24	1	X2	S
793-5982-001	14 - 88	1	X2	S
793-5987-002	14 - 30	1	X2	S
793-5988-001	14 - 28	1	X2	S
793-5989-002	14 - 23	1	X2	S
793-5990-001	14 - 21	1	X2	S
793-5993-002	14 - 28	1	X2	S
793-5994-001	14 - 26	1	X2	S
793-5997-002	14 - 40	1	X2	S
793-5998-001	14 - 38	1	X2	S
793-6000-002	14 - 32	1	X2	S
793-6001-001	14 - 30	1	X2	S
793-6012-002	14 - 94	1	X2	S
793-6012-003	14 - 93	1	X2	S
793-6013-001	14 - 80	1	A1	D
793-6037-002	14 - 76	1	X2	S
793-6041-001	14 - 64	1	X2	S
793-6044-001	14 - 1	1	X2	S
793-6052-001	14 - 86	1	X2	S
793-6249-001	2 -104	14	X2	S
	13 - 97			
	14 - 85			
793-6256-001	14 - 81	1	X1	S
793-8982-001	2 - 11	1	P1	D
	8 - 20			
793-9260-001	2 - 6	2	P1	D
	3 -106			
	13 - 8			
793-9305-001	2 - 47	2	P1	D
	10 - 16			
	13 - 43			
793-9321-001	10 - 5	1	P1	F
	11 - 14			
793-9322-001	10 - 7	1	P1	D
	12 - 28			
795-5243-001	13 - 18	1	P1	S
795-5244-001	2 - 21	1	P1	S
795-5245-001	2 - 22	2	X1	S
	13 - 19			
795-5246-001	2 - 58H	4	M1	S
	13 - 55			
795-8756-001	2 - 99A	1	M	S
795-8757-001	2 - 52	1	M	S
795-8758-001	13 - 75	1	M	S
795-8759-001	13 - 47	1	M	S
795-8763-000	1 - 1	1		
795-8763-001	1 - 1	1	X2	S
795-8764-001	13 - 1	2	X2	S
	13 - 1			
795-8765-000	2 - 1	1		
795-8765-001	2 - 1	1	X2	S
795-8766-000	14 - 79	1		
795-8766-001	14 - 79	1	X2	S
796-1260-001	14 - 24	1	X2	S
9261	7 - 1	1	P1	S
953-1208-400	12 - 9	1	P1	S

SECTION IV
REFERENCE DESIGNATION INDEX

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A1	14-19	783-1427-001
A1	15-	783-1472-001
A1R1	15- 3	RNC60H5900FR
A1R2	15- 3	RNC60H5900FR
A1R21	15- 5	RNC60H9090FR
A1R22	15- 5	RNC60H9090FR
A1R23	15- 5	RNC60H9090FR
A1R24	15- 5	RNC60H9090FR
A1R25	15- 5	RNC60H9090FR
A1R26	15- 4	RNC60H7150FR
A1R27	15- 4	RNC60H7150FR
A1R28	15- 4	RNC60H7150FR
A1R29	15- 4	RNC60H7150FR
A1R3	15- 3	RNC60H5900FR
A1R30	15- 4	RNC60H7150FR
A1R31	15- 4	RNC60H7150FR
A1R32	15- 4	RNC60H7150FR
A1R33	15- 4	RNC60H7150FR
A1R34	15- 4	RNC60H7150FR
A1R35	15- 4	RNC60H7150FR
A1R36	15- 3	RNC60H5900FR
A1R37	15- 2	RNC60H3010FR
A1R38	15- 2	RNC60H3010FR
A1R39	15- 2	RNC60H3010FR
A1R4	15- 3	RNC60H5900FR
A1R40	15- 2	RNC60H3010FR
A1R44	15- 6	RNC60H9530FR
A1R5	15- 3	RNC60H5900FR
A1R6	15- 3	RNC60H5900FR
A1R7	15- 3	RNC60H5900FR
A1R8	15- 3	RNC60H5900FR
A2	14-11	TLC333C
A3	14-14	TLC213MOD
A4	14-12	TLC555C
A5	14-13	TLC444C
A5	14-11	TLC333C
A6	14-14A	TLC444C
A7	1- 2	787-6487-001
A7	2-	787-6487-001
A7A1	2- 6	793-9260-001
A7A1	3-	793-9260-001
A7A1A1	3- 7	351-7437-012
A7A1A10	3- 1	54L00SD7722A
A7A1A11	3- 5	SD9857A
A7A1A12	3- 1	54L00SD7722A
A7A1A13	3- 2	54L10SD7723A
A7A1A14	3- 6	UD4225
A7A1A15	3- 1	54L00SD7722A
A7A1A16	3- 1	54L00SD7722A
A7A1A17	3- 1	54L00SD7722A

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A7A1A24	3- 2	54L10SD7723A
A7A1A25	3- 3	54L20SD7724A
A7A1A26	3- 5	SD9857A
A7A1A3	3- 4	54L73SD8545A
A7A1A4	3- 1	54L00SD7722A
A7A1A5	3- 6	UD4225
A7A1A6	3- 5	SD9857A
A7A1A7	3- 1	54L00SD77SSA
A7A1A8	3- 2	54L10SD7723A
A7A1A9	3- 6	US4225
A7A1CR1	3- 13	353-3338-001
A7A1CR2	3- 12	353-2978-001
A7ACR3	3- 13	353-3338-001
A7A1C1	3- 30	CK078X221K
A7A1C10	3- 31	CK32BV104M
A7A1C11	3- 29	G544BX152M
A7A1C12	3- 33	CSR13D226KM
A7A1C2	3- 30	CK078X221K
A7A1C3	3- 32	M39003-01-2117
A7A1C4	3- 31	CK32BV104M
A7A1C5	3- 31	CK32BV104M
A7A1C6	3- 31	CK32BV104M
A7A1C7	3- 31	CK32BV104M
A7A1C8	3- 31	CK32BV104M
A7A1C9	3- 31	CK32BV104M
A7A1P1	3- 15	372-2621-021
A7A1P2	3- 14	372-2623-045
A7AQ1	3- 9	352-7500-191
A7AQ2	3- 9	352-7500-191
A7AQ3	3- 9	352-7500-191
A7AQ4	3- 10	352-7500-281
A7AQ5	3- 10	352-7500-281
A7A1R1	3- 18	RCR07G100KS
A7A1R10	3- 28	RCR05G103K
A7A1R11	3- 22	RCR05G682JS
A7A1R12	3- 28	RCR05G103K
A7A1R13	3- 28	RCR05G103K
A7A1R14	3- 28	RCR05G103K
A7A1R15	3- 28	RCR05G103K
A7A1R16	3- 28	RCR05G103K
A7A1R17	3- 28	RCR05G103K
A7A1R18	3- 28	RCR05G103K
A7A1R19	3- 28	RCR05G103K
A7A1R2	3- 25	RCR05G222K
A7A1R20	3- 28	RCR05G103K
A7A1R21	3- 24	RCR05G102K
A7A1R22	3- 28	RCR05G103K
A7A1R23	3- 28	RCR05G103K
A7A1R24	3- 26	RCR05G472K
A7A1R25	3- 26	RCR05G472K

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A7A1R26	3-26	RCR05G472k
A7A1R27	3-28	RCR05G103K
A7A1R28	3-28	RCR05G103K
A7A1R29	3-28	RCR05G103K
A7A1R30	3-28	RCR05G103K
A7A1R31	3-28	RCR05G103K
A7A1R32	3-28	RCR05G103K
A7A1R33	3-21A	RCR05G512JS
A7A1R34	3-21	RCR05G432JS
A7A1R35	3-20	RCR05G332JS
A7A1R36	3-24	RCR05G102K

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A7A1R37	3 - 19	RCR05G272JS
A7A1R38	3 - 28	RCR05G103K
A7A1R39	3 - 28	RCR05G103K
A7A1R4	3 - 25	RCR05G222K
A7A1R40	3 - 23	RCR05G103JS
A7A1R41	3 - 23	RCR05G103JS
A7A1R42	3 - 27	RCR05G822K
A7A1R5	3 - 18	RCR07G100KS
A7A1R6	3 - 25	RCR05G222K
A7A1R8	3 - 25	RCR05G222K
A7A1R9	3 - 22	RCR05G682JS
A7A1O	2 -	789-2596-001
A7A1OJ1	2 - 30	JTP02RE16-55P014
A7A1OJ2	2 - 38	JTP02RE12-98P014
A7A1OJ3	2 - 43	JTP02RE14-37S
A7A1OPS1	2 - 47	793-9305-001
A7A1OPS1	10 -	793-9305-001
A7A1OPS1A1	10 - 5	793-9321-001
A7A1OPS1A1	11 -	793-9321-001
A7A1OPS1A1CR10-CR1	11 - 23	353-3337-001
A7A1OPS1A1CR17	11 - 3	353-9008-011
A7A1OPS1A1CR18	11 - 3	353-9008-011
A7A1OPS1A1CR19	11 - 3	353-9008-011
A7A1OPS1A1CR20	11 - 3	353-9008-011
A7A1OPS1A1CR21	11 - 4	353-3625-011
A7A1OPS1A1CR22	11 - 4	353-3625-011
A7A1OPS1A1CR23	11 - 3	353-9008-011
A7A1OPS1A1CR9	11 - 23	353-3337-001
A7A1OPS1A1C13	11 - 21	M39003-01-2062
A7A1OPS1A1C14	11 - 21	M39003-01-2062
A7A1OPS1A1C15-C18	11 - 22	M39003-01-2140
A7A1OPS1A1C20	11 - 27	M39003-01-2047
A7A1OPS1A1C21	8 - 12	54L73SN14834
A7A1OPS1A1C22	11 - 6	M39003-01-2005
A7A1OPS1A1C25	11 - 25	CK05BX470K
A7A1OPS1A1C26	11 - 25	CK05BX470K
A7A1OPS1A1L3	11 - 19	MS90537-41
A7A1OPS1A1L4	11 - 20	MS90537-30
A7A1OPS1A1L7	11 - 20	MS90537-30
A7A1OPS1A1P1	11 - 18	372-2625-017
A7A1OPS1A1P2	11 - 18	372-2625-017
A7A1OPS1A1P3	11 - 17	372-2624-011
A7A1OPS1A1Q10	11 - 1	352-7500-281
A7A1OPS1A1Q11	11 - 1	352-7500-281
A7A1OPS1A1Q4	11 - 2	352-7500-191
A7A1OPS1A1Q5	11 - 2	352-7500-191
A7A1OPS1A1Q6	11 - 2	352-7500-191
A7A1OPS1A1Q7	11 - 2	352-7500-191
A7A1OPS1A1Q8	11 - 1	352-7500-281
A7A1OPS1A1Q9	11 - 1	352-7500-281
A7A1OPS1A1R10	11 - 5	RT22C2P101
A7A1OPS1A1R11	11 - 14	RCR07G820KS
A7A1OPS1A1R12	11 - 8	RNC60H1000FR
A7A1OPS1A1R13	11 - 7	RCR07G103KS
A7A1OPS1A1R14	11 - 9	RNC60H1101FR
A7A1OPS1A1R15	11 - 7	RCR07G103KS
A7A1OPS1A1R16	11 - 15	RCR07G22CKS
A7A1OPS1A1R17	11 - 15	RCR07G220KS
A7A1OPS1A1R18	11 - 10	RNC60H7500FR
A7A1OPS1A1R19	11 - 13	RCR07G221KS
A7A1OPS1A1R20	11 - 5	RT22C2P101
A7A1OPS1A1R21	11 - 12	RNC60H5620FR
A7A1OPS1A1R22	11 - 11	RNC60H5110
A7A1OPS1A1R23	11 - 8	RNC60H1000
A7A1OPS1A1R27	10 - 7	RCR07G103KS
A7A1OPS1A1R28	11 - 26	RCR07G682KS
A7A1OPS1A1R29	11 - 10A	RN6CD1961F
A7A1OPS1A1R6	11 - 10	RNC60H7500FR
A7A1OPS1A1R7	11 - 13	RCR07G221KS
A7A1OPS1A1R8	11 - 11	RNC60H5110FR
A7A1OPS1A1R9	11 - 11	RNC60H5110FR
A7A1OPS1A2	10 - 7	793-9322-001
A7A1OPS1A2	12 -	793-9322-001
A7A1OPS1A2CR1	12 - 16	353-9009-061
A7A1OPS1A2CR2	12 - 16	353-9009-061
A7A1OPS1A2CR3	12 - 16	353-9009-061
A7A1OPS1A2CR4	12 - 16	353-9009-061
A7A1OPS1A2CR5-CR8	11 - 4	353-9009-011
A7A1OPS1A2C1	12 - 18	M39018-01-0276
A7A1OPS1A2C10	12 - 8	M39003-01-2026
A7A1OPS1A2C11	12 - 8	M39003-01-2026
A7A1OPS1A2C12	12 - 8	M39003-01-2026
A7A1OPS1A2C19	12 - 6	CK63AW103M
A7A1OPS1A2C2	12 - 18	M39018-01-0276
A7A1OPS1A2C23	12 - 7	41C92
A7A1OPS1A2C24	12 - 18	M39018-01-0276
A7A1OPS1A2C27-C30	12 - 3A	CM05FD391JP3
A7A1OPS1A2C3	12 - 18	M39018-01-0276
A7A1OPS1A2C4	12 - 18	M39018-01-0276
A7A1OPS1A2C5	12 - 7	41C92

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A7A1OPS1A2C6	12 - 7	41C92
A7A1OPS1A2C8	12 - 3	CK63CZ332M
A7A1OPS1A2C9	12 - 8	M39003-01-2026
A7A1OPS1A2L2	12 - 9	953-1208-400
A7A1OPS1A2L5	12 - 12	MS91189-30
A7A1OPS1A2L6	12 - 12	MS91189-30
A7A1OPS1A2Q1	12 - 15	352-7500-491
A7A1OPS1A2Q2	12 - 15	352-7500-491
A7A1OPS1A2Q3	12 - 5	353-6080-001
A7A1OPS1A2R1	12 - 1	RW69V2R7
A7A1OPS1A2R2	12 - 17	RW69V1R8
A7A1OPS1A2R26	12 - 20	RCR07G102KS
A7A1OPS1A2R29	12 - 20	RCR07G102KS
A7A1OPS1A2R4	12 - 2	RW69V151
A7A1OPS1A2R5	12 - 1	RW69V2R7
A7A1OPS1A2T1	12 - 13	3-18536
A7A1OPS1CR24	10 - 8A	353-2852-001
A7A1OPS1CR24	10 - 8A	1N647
A7A1OPS1L1	10 - 9	3-18572
A7A1OPS1R24	10 - 9A	RH5X000B10001F
A7A1OS1	2 - 29	MS75028-23
A7A2	2 - 7	633-9332-001
A7A2	2 - 7	789-2620-001
A7A2	4 -	789-2620-001
A7A2A1	4 - 11	H08014S
A7A2A10	4 - 7	HL11561
A7A2A11	4 - 15	G371K2
A7A2A12	4 - 1	F51K2
A7A2A13	4 - 3	54L00SD7722A
A7A2A14	4 - 16	HL30110
A7A2A15	4 - 6	SN19670
A7A2A16	4 - 2	SS314
A7A2A17	4 - 8	351-7436-012
A7A2A18	4 - 7	HL11561
A7A2A19	4 - 7	HL11561
A7A2A2	4 - 13	H12014S
A7A2A20	4 - 4	54L20SD7724A
A7A2A21	4 - 6	SN19670
A7A2A22	4 - 2	SS314
A7A2A23	4 - 8	351-7436-012
A7A2A24	4 - 7	HL11561
A7A2A25	4 - 7	HL11561
A7A2A26	4 - 1	F51K2
A7A2A27	4 - 5	SD9857A
A7A2A28	4 - 2	SS314
A7A2A29	4 - 8	351-7436-012
A7A2A3	4 - 9	H10004S
A7A2A30	4 - 7	HL11561
A7A2A31	4 - 7	HL11561
A7A2A4	4 - 16	HL30110
A7A2A5	4 - 12	H08015S
A7A2A6	4 - 14	H12015S
A7A2A7	4 - 10	H10005S
A7A2A8	4 - 15	G371K2
A7A2A9	4 - 7	HL11561
A7A2CR1	4 - 19	353-2978-001
A7A2CR1	4A- 13	353-2850-001
A7A2CR2	4 - 20	353-3338-001
A7A2CR3	4 - 19	353-2978-001
A7A2C1	4 - 29	CK32BV104M
A7A2C1	4A- 17	M39003-01-2296
A7A2C2	4 - 29	CK32BV104M
A7A2C2-C13	4A- 2	CKR05BX104MM
A7A2C3	4 - 28	G544BX182J
A7A2C4	4 - 29	CK32BV104M
A7A2P1	4 - 22	372-2623-045
A7A2P1	4A- 19	372-2623-045
A7A2P2	4 - 21	372-2621-013
A7A2P2	4A- 6	372-2621-013
A7A2Q1	4 - 18	352-7500-281
A7A2R1	4 - 30	RNR55J2611FM
A7A2R1	4A- 14	RCR05G223JS
A7A2R10	4 - 25	RNR55J1002FM
A7A2R15	4A- 3	RCR05G102KS
A7A2R2	4 - 27	RCR05G472K
A7A2R2	4A- 12	RCR05G102JS
A7A2R3	4 - 27	RCR05G472K
A7A2R3-R6	4A- 3	RCR05G102KS
A7A2R4	4 - 27	RCR05G472K
A7A2R5	4 - 26	RNR55J2492FM
A7A2R6	4 - 25	RNR55J1002FM
A7A2R7	4 - 27	RCR05G472K
A7A2R7-R14	4A- 11	RCR05G103KS
A7A2R8	4 - 27	RCR05G472K
A7A2R9	4 - 27	RCR05G472K
A7A2U11	4A- 10	AM25S80DMB0037
A7A2U21	4A- 9	AM27S80DMB0036
A7A2U31	4A- 15	SNC54LS251J
A7A2U?	4A- 4	351-1605-011
A7A2U?	4A- 4	351-1605-011

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A7A2U41	4A- 16	351-1523-032
A7A2U42	4A- 8	SNC54LS91J
A7A2U43	4A- 4	351-1605-011
A7A2U51	4A- 16	351-1523-032
A7A2U52	4A- 9	SNC54LS91J
A7A2U53	4A- 4	351-1605-011
A7A2U61	4A- 18	M38510-02002BCB
A7A2U62	4A- 7	M38510-02004BCB
A7A2U63	4A- 5	SNC54LS76J
A7A2U71	4A- 5	SNC54LS76J
A7A2U72	4A- 5	SNC54LS76J
A7A3	2 - 8	789-2618-001
A7A3	5 -	789-2618-001
A7A3A1	5 - 4	54L00SD7722A
A7A3A10	5 - 5	54L10SD7723A
A7A3A11	5 - 5	54L10SD7723A
A7A3A12	5 - 5	54L10SD7723A
A7A3A13	5 - 4	54LC0SD7722A
A7A3A14	5 - 9	12397-93C151
A7A3A15	5 - 8	54L73SD8545A
A7A3A16	5 - 2	F51K2
A7A3A17	5 - 4	54LC0SD7722A
A7A3A18	5 - 4	54LC0SD7722A
A7A3A19	5 - 4	54LC0SD7722A
A7A3A2	5 - 3	SF10112
A7A3A20	5 - 5	54L10SD7723A
A7A3A21	5 - 8	54L73SD8545A
A7A3A22	5 - 8	54L73SD8545A
A7A3A23	5 - 4	54L00SD7722A
A7A3A24	5 - 7	54L30SD7725A
A7A3A25	5 - 4	54L00SD7722A
A7A3A26	5 - 5	54L10SD7723A
A7A3A27	5 - 8	54L73SD8545A
A7A3A28	5 - 1	G191K2
A7A3A29	5 - 4	54L00SD7722A
A7A3A3	5 - 3	SF10112
A7A3A30	5 - 4	54L00SD7722A
A7A3A31	5 - 4	54LC0SD7722A
A7A3A32	5 - 4	54L00SD7722A
A7A3A33	5 - 6	54L20SD7724A
A7A3A34	5 - 8	54L73SD8545A
A7A3A35	5 - 6	54L20SD7724A
A7A3A36	5 - 8	54L73SD8545A
A7A3A37	5 - 6	54L20SD7724A
A7A3A4	5 - 3	SF10112
A7A3A5	5 - 4	54L00SD7722A
A7A3A6	5 - 10	HL11554
A7A3A7	5 - 3	SF10112
A7A3A8	5 - 3	SF10112
A7A3A9	5 - 5	54L10SD7723A
A7A3C1	5 - 18	CK32BV104M
A7A3C2	5 - 18	CK32BV104M
A7A3C3	5 - 17	CK31BT102K
A7A3P1	5 - 12	372-2621-045
A7A3P2	5 - 11	372-2621-014
A7A3R1	5 - 14	RCR05G331K
A7A3R2	5 - 15	RCR05G471K
A7A3R3	5 - 16	RCR05G821K
A7A3R4	5 - 15	RCR05G471KS
A7A3R5	5 - 15	RCR05G471KS
A7A3R6	5 - 16	RCR05G821KS
A7A4	2 - 9	789-2622-001
A7A4	6 -	789-2622-001
A7A4A1	6 - 5	F51K2
A7A4A10	6 - 8	54LC0SD7722A
A7A4A12	6 - 6	SF10112
A7A4A13	6 - 12	351-7436-012
A7A4A14	6 - 13	G371K2
A7A4A15	6 - 9	54L10SD7723A
A7A4A16	6 - 4	G191K2
A7A4A17	6 - 6	SF10112
A7A4A18	6 - 12	351-7436-012
A7A4A19	6 - 8	54L00SD7722A
A7A4A2	6 - 11	54L72SD7730A
A7A4A20	6 - 8	54L00SD7722A
A7A4A21	6 - 5	F51K2
A7A4A22	6 - 13	G371K2
A7A4A23	6 - 10	54L20SD7724A
A7A4A24	6 - 6	SF10112
A7A4A25	6 - 6	SF10112
A7A4A26	6 - 8	54LC0SD7722A
A7A4A27	6 - 3	SG14127
A7A4A3	6 - 8	54L00SD7722A
A7A4A4	6 - 9	54L10SD7723A
A7A4A5	6 - 10	54L20SD7724A
A7A4A6	6 - 8	54LC0SD7722A
A7A4A7	6 - 7	SG8025
A7A4A7	6 - 8	54L00SD7722A
A7A4A8	6 - 13	G371K2
A7A4A9	6 - 2	G14CK2

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A7A4CR1	6 - 18	353-3338-001
A7A4CR1	6 - 18	353-2906-001
A7A4CR2	6 - 17	353-2710-001
A7A4CR2	6 - 17	353-2978-001
A7A4C1	6 - 35	CK31BV513K
A7A4C10	6 - 37	CSR13D226KM
A7A4C2	6 - 32	G544BX182J
A7A4C3	6 - 31	G544BX152M
A7A4C4	6 - 33	CK07BX470K
A7A4C4	6 - 33	G544BX470J
A7A4C5	6 - 34	CK07BX561K
A7A4C5	6 - 34	G544BX561J
A7A4C6	6 - 36	CK32BV104M
A7A4C7	6 - 36	CK32BV104M
A7A4C8	6 - 36	CK32BV104M
A7A4C9	6 - 36	CK32BV104M
A7A4L1	6 - 1	MS90537-45
A7A4P1	6 - 19	372-2621-045
A7A4P2	6 - 19A	372-2621-015
A7A4Q1	6 - 15	352-0661-041
A7A4Q2	6 - 15	352-0661-041
A7A4Q3	6 - 15	352-0661-041
A7A4Q4	6 - 16	352-7500-781
A7A4Q4	6 - 16	352-0551-041
A7A4R1	6 - 30	RCR05G103K
A7A4R10	6 - 23	RCR05G432JS
A7A4R10	6 - 23	RCR07G392JS
A7A4R11	6 - 23	RCR05G432JS
A7A4R11	6 - 23	RCR07G392JS
A7A4R12	6 - 22	RCR05G332JS
A7A4R12	6 - 22	RCR07G362JS
A7A4R13	6 - 27	RCR05G102K
A7A4R14	6 - 29	RCR05G822K
A7A4R15	6 - 17	RCR05G682K
A7A4R2	6 - 28	RCR05G472K
A7A4R3	6 - 21	RCR05G102JS
A7A4R4	6 - 25	RCR05G333JS
A7A4R5	6 - 26	RCR05G151K
A7A4R6	6 - 27	RCR05G102K
A7A4R7	6 - 24	RCR05G562JS
A7A4R8	6 - 28	RCR05G472K
A7A4R9	6 - 28	RCR05G472K
A7A5	2 - 10	789-2624-001
A7A5	7 -	789-2624-001
A7A5A1	7 - 6	54L00SD7722A
A7A5A10	7 - 7	54L10SD7723A
A7A5A11	7 - 11	HL11554
A7A5A12	7 - 4	SS314
A7A5A13	7 - 12	351-7437-012
A7A5A14	7 - 6	54L00SD7722A
A7A5A15	7 - 1	9261
A7A5A16	7 - 2	SG14127
A7A5A17	7 - 6	54L00SD7722A
A7A5A18	7 - 8	SD7727A
A7A5A19	7 - 3	SG812
A7A5A2	7 - 10	54L73SD8545A
A7A5A20	7 - 13	G371K2
A7A5A21	7 - 13	G371K2
A7A5A22	7 - 8	SD7727A
A7A5A23	7 - 8	SD7727A
A7A5A24	7 - 6	54L00SD7722A
A7A5A25	7 - 6	54L00SD7722A
A7A5A26	7 - 6	54L00SD7722A
A7A5A27	7 - 6	54L00SD7722A
A7A5A28	7 - 8	SD7727A
A7A5A29	7 - 6	54L00SD7722A
A7A5A3	7 - 7	54L10SD7723A
A7A5A30	7 - 8	SD7727A
A7A5A31	7 - 5	SM2014
A7A5A32	7 - 6	54L00SD7722A
A7A5A33	7 - 9	54L72SD7730A
A7A5A4	7 - 6	54L00SD7722A
A7A5A5	7 - 6	54L00SD7722A
A7A5A6	7 - 4	SS314
A7A5A7	7 - 4	SS314
A7A5A8	7 - 4	SS314
A7A5A9	7 - 4	SS314
A7A5C1	7 - 19	CK32BV104M
A7A5C2	7 - 19	CK32BV104M
A7A5C3	7 - 19	CK32BV104M
A7A5C4	7 - 18	CK07BX181K
A7A5C4	7 - 18	G544BX181M
A7A5C5	7 - 18	CK07BX181K
A7A5C5	7 - 18	G544BX181M
A7A5P1	7 - 15	372-2623-045
A7A5P2	7 - 14	372-2621-014
A7A6	2 - 11	793-8982-001
A7A6	8 -	793-8982-001
A7A6A1	8 - 11	SD7726A
A7A6A10	8 - 13	SM7037A

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A7A6A11	8 - 8	54L00SD7722A
A7A6A12	8 - 20	G371K2
A7A6A13	8 - 9	54L10SD7723A
A7A6A14	8 - 12	54L73SD8545A
A7A6A15	8 - 18	A7K37051422A
A7A6A16	8 - 13	SM7C37A
A7A6A17	8 - 13	SM7C37A
A7A6A18	8 - 19	G380K2
A7A6A19	8 - 8	54L00SD7722A
A7A6A2	8 - 14	HL11561
A7A6A20	8 - 10	54L20SD7724A
A7A6A21	8 - 15	12483
A7A6A22	8 - 13	SM7C37A
A7A6A23	8 - 17	351-7445-012
A7A6A24	8 - 9	54L10SD7723A
A7A6A25	8 - 7	SG14127
A7A6A26	8 - 8	54L00SD7722A
A7A6A27	8 - 18	A7K37051422A
A7A6A28	8 - 13	SM7C37A
A7A6A29	8 - 13	SM7C37A
A7A6A3	8 - 14	HL11561
A7A6A30	8 - 18	A7K37051422A
A7A6A31	8 - 13	SM7C37A
A7A6A32	8 - 5	351-0025-010
A7A6A33	8 - 4	351-0024-010
A7A6A34	8 - 6	351-2022-010
A7A6A4	8 - 13	SM7C37A
A7A6A5	8 - 16	351-7436-012
A7A6A6	8 - 11	SD7726A
A7A6A7	8 - 20	G371K2
A7A6A8	8 - 12	54L73SD8545A
A7A6A8	13 - 38	JTPC2RE14-37S014
A7A6A9	8 - 18	A7K37051422A
A7A6CR1	8 - 21	353-9010-261
A7A6CR1	8 - 21	353-6522-041
A7A6CR2	8 - 22	353-9010-201
A7A6CR2	8 - 22	353-3129-001
A7A6C1	8 - 41	CK07BX561K
A7A6C1	8 - 41	G544BX152M
A7A6C10	8 - 12A	CK05BX222K
A7A6C2	8 - 2	CSR13D226KM
A7A6C3	8 - 42	CK31BT392K
A7A6C4	8 - 1	CSR13C475MM
A7A6C5	8 - 3	CSR13G393KM
A7A6C6	8 - 2	CSR13D226KM
A7A6C7	8 - 43	CK32BV104M
A7A6C8	8 - 43	CK32BV104M
A7A6C9	8 - 2	CSR13D226KM
A7A6P1	8 - 24	372-2623-045
A7A6R1	8 - 37	RCR05G223K
A7A6R10	8 - 37	RCR05G223K
A7A6R11	8 - 34	RCR05G272K
A7A6R12	8 - 35	RCR05G472K
A7A6R13	8 - 36	RCR05G103K
A7A6R14	8 - 31	RCR05G682JS
A7A6R15	8 - 37	RCR05G223K
A7A6R16	8 - 35	RCR05G422K
A7A6R17	8 - 37	RCR05G223K
A7A6R18	8 - 37	RCR05G223K
A7A6R19	8 - 37	RCR05G223K
A7A6R2	8 - 37	RCR05G223K
A7A6R20	8 - 37	RCR05G223K
A7A6R21	8 - 37	RCR05G223K
A7A6R22	8 - 37	RCR05G223K
A7A6R23	8 - 37	RCR05G223K
A7A6R24	8 - 30	RCR05G561JS
A7A6R25	8 - 28	RCR05G910JS
A7A6R26	8 - 30	RCR05G561JS
A7A6R27	8 - 39	RNR55J2872FM
A7A6R27	8 - 39	RNR55J2742FM
A7A6R27	8 - 39	RNR55J2802FM
A7A6R27	8 - 39	RNR55J2942FM
A7A6R27	8 - 39	RNR55J3012FM
A7A6R27	8 - 39	RNR55J3092FM
A7A6R27	8 - 39	RNR55J3162FM
A7A6R27	8 - 39	RNR55J3242FM
A7A6R27	8 - 39	RNR55J3322FM
A7A6R28	8 - 34	RCR05G272K
A7A6R29	8 - 29	RCR05G471JS
A7A6R3	8 - 34	RCR05G272K
A7A6R30	8 - 29	RCR05G471JS
A7A6R31	8 - 40	RNR55J6492FM
A7A6R31	8 - 40	RNR55J6652FM
A7A6R31	8 - 40	RNR55J6812FM
A7A6R31	8 - 40	RNR55J6982FM
A7A6R31	8 - 40	RNR55J7152FM
A7A6R31	8 - 40	RNR55J7322FM
A7A6R31	8 - 40	RNR55J7502FM
A7A6R31	8 - 40	RNR55J7682FM
A7A6R31	8 - 40	RNR55J7872FM

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A7A6R32	8 - 40	RNR55J6492FM
A7A6R32	8 - 40	RNR55J6652FM
A7A6R32	8 - 40	RNR55J6812FM
A7A6R32	8 - 40	RNR55J6982FM
A7A6R32	8 - 40	RNR55J7152FM
A7A6R32	8 - 40	RNR55J7322FM
A7A6R32	8 - 40	RNR55J7502FM
A7A6R32	8 - 40	RNR55J7682FM
A7A6R32	8 - 40	RNR55J7872FM
A7A6R33	8 - 38	RCR05G681JS
A7A6R33	8 - 38	RCR05G102JS
A7A6R33	8 - 38	RCR05G152JS
A7A6R33	8 - 38	RCR05G222JS
A7A6R33	8 - 38	RCR05G332JS
A7A6R33	8 - 38	RCR05G392JS
A7A6R33	8 - 38	RCR05G472JS
A7A6R33	8 - 38	RCR05G562JS
A7A6R33	8 - 38	RCR05G682JS
A7A6R33	8 - 38	RCR05G822JS
A7A6R33	8 - 38	RCR05G103JS
A7A6R33	8 - 38	RCR05G123JS
A7A6R33	8 - 38	RCR05G153JS
A7A6R33	8 - 38	RCR05G183JS
A7A6R33	8 - 38	RCR05G223JS
A7A6R33	8 - 38	RCR05G273JS
A7A6R33	8 - 38	RCR05G333JS
A7A6R34	8 - 29	RCR05G471JS
A7A6R35	8 - 33	RCR05G680K
A7A6R36	8 - 32	RCR05G103JS
A7A6R4	8 - 34	RCR05G272K
A7A6R5	8 - 34	RCR05G272K
A7A6R6	8 - 37	RCR05G223K
A7A6R7	8 - 37	RCR05G223K
A7A6R8	8 - 37	RCR05G223K
A7A6R9	8 - 37	RCR05G223K
A7A6TP1	8 - 23	372-2621-013
A7A6T1	8 - 27	317-187
A7A6T2	8 - 27	317-187
A7A6T3	8 - 27	317-187
A7A7	2 - 12	789-2612-001
A7A7	9 -	789-2612-001
A7A7A1	9 - 3	54L00SD7722A
A7A7A10	9 - 5	54L30SD7725A
A7A7A11	9 - 3	54L00SD7722A
A7A7A12	9 - 4	54L20SD7724A
A7A7A13	9 - 3	54L00SD7722A
A7A7A14	9 - 2	SG14127
A7A7A15	9 - 3	54L00SD7722A
A7A7A16	9 - 2	SG14127
A7A7A17	9 - 3	54L00SD7722A
A7A7A2	9 - 6	SD9857A
A7A7A3	9 - 6	SD9857A
A7A7A4	9 - 6	SD9857A
A7A7A5	9 - 3	54L00SD7722A
A7A7A6	9 - 6	SD9857A
A7A7A7	9 - 6	SD9857A
A7A7A8	9 - 6	SD9857A
A7A7A9	9 - 3	54L00SD7722A
A7A7CR1-CR70	9 - 7	353-3656-031
A7A7C1	9 - 14	CK31BT102K
A7A7C1	9 - 14	CK31BT102M
A7A7C10	9 - 1	CSR13D226MM
A7A7C11	9 - 15	CK32BV104M
A7A7C12	9 - 15	CK32BV104M
A7A7C13	9 - 15	CK32BV104M
A7A7C14	9 - 15	CK32BV104M
A7A7C15	9 - 15	CK32BV104M
A7A7C16	9 - 15	CK32BV104M
A7A7C17	9 - 15	CK32BV104M
A7A7C18	9 - 14	CK31BT102K
A7A7C18	9 - 14	CK31BT102M
A7A7C19	9 - 14	CK31BT102K
A7A7C19	9 - 14	CK31BT102M
A7A7C2	9 - 14	CK31BT102K
A7A7C2	9 - 14	CK31BT102M
A7A7C20	9 - 14	CK31BT102K
A7A7C20	9 - 14	CK31BT102M
A7A7C21	9 - 14	CK31BT102K
A7A7C21	9 - 14	CK31BT102M
A7A7C3	9 - 14	CK31BT102K
A7A7C3	9 - 14	CK31BT102M
A7A7C4	9 - 14	CK31BT102K
A7A7C4	9 - 14	CK31BT102M
A7A7C5	9 - 14	CK31BT102K
A7A7C5	9 - 14	CK31BT102M
A7A7C6	9 - 14	CK31BT102K
A7A7C6	9 - 14	CK31BT102M
A7A7C7	9 - 14	CK31BT102K
A7A7C7	9 - 14	CK31BT102M
A7A7C8	9 - 14	CK31BT102K

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A7A7C8	9 - 14	CK31BT102M
A7A7C9	9 - 15	CK32BV104M
A7A7P1	9 - 11	M21097-1-136
A7A7R1-R24	9 - 13	RCR05G104JS
A7A7R25-R31	9 - 12	RCR05G103JS
A7A7TP1	9 - 9	M39024-11-04
A7A7TP2	9 - 8	M39024-11-03
A7A8	2 - 56	789-2626-001
A7A9	2 -	789-2594-001
A7A9DS1	2 - 77	5160-458-604RED
A7A9DS2	2 - 76	5160-458-604GRN
A7A9DS3	2 - 76	5160-458-604GRN
A7A9DS4	2 - 76	5160-458-604GRN
A7A9DS5	2 - 76	5160-458-604GRN
A7A9DS6	2 - 62	381
A7A9J1	2 - 90	130GOLD
A7A9P1	2 - 95	789-2653-001
A7A9P2	2 - 94	789-2652-001
A7A9R1	2 - 91	M22-01-00091SB
A7A9S1	2 - 84	259-2769-050
A7A9S10	2 - 68	7C36
A7A9S11	2 - 66	183-0101-1474-60
A7A9S2	2 - 89	MS90311-211
A7A9S3	2 - 78	259-2769-030
A7A9S4	2 - 87	W1046
A7A9S5	2 - 73	259-2769-010
A7A9S6	2 - 73	259-2769-010
A7A9S7	2 - 81	259-2769-090
A7A9S8	2 - 73	259-2769-010
A7A9S9	2 - 73	259-2769-010
A8	1 - 3	787-6444-001
A8	13 -	787-6444-001
A8A1	SAME AS	A7A1
A8A1	13 - 8	793-9260-001
A8A2	SAME AS	A7A7
A8A2	13 - 9	789-2612-001
A8A3	13 - 53	789-2626-001
A8A4	13 -	789-2591-001
A8A4DS1	13 - 79	5160-458-604RED
A8A4DS2	13 - 80	5160-458-604GRN
A8A4DS3	13 - 80	5160-458-604GRN
A8A4DS4	13 - 80	5160-458-604GRN
A8A4DS5	13 - 59	381
A8A4J1	13 - 81	130GOLD
A8A4P1	13 - 88	789-2652-001
A8A4P2	13 - 87	789-2653-001
A8A4R1	13 - 84	M22-01-00091SB
A8A4S1	13 - 76	259-2769-010
A8A4S10	13 - 65	7C36
A8A4S11	13 - 63	183-0101-1474-60
A8A4S2	13 - 73	259-2769-020
A8A4S3	13 - 73	259-2769-020
A8A4S4	13 - 82	W1046
A8A4S5	13 - 70	259-2769-060
A8A4S6	13 - 70	259-2769-060
A8A4S7	13 - 70	259-2769-060
A8A4S8	13 - 70	259-2769-060
A8A4S9	13 - 70	259-2769-060
A8A5	13 -	789-2593-001
A8A5J2	13 - 25	JTP02RE16-55P014
A8A5J3	13 - 33	JTP02RE12-98P014
A8A5PS1	SAME AS	A7A10PS1
A8A5PS1	13 - 43	793-9305-001
CB1	14 - 70	APL-328-110
C1	14 - 38A	CP09A1KC224K3
DS1	14 - 54	MS24515-685
DS2	14 - 54	MS24515-685
DS3	14 - 54	MS24515-685
DS4	14 - 54	MS24515-685
DS5	14 - 54	MS24515-685
FL1	14 - 16	4JX14
FL2	14 - 16	4JX14
FL3	14 - 10	JW33-1114A
FL4	14 - 10	JW33-1114A
FL5	14 - 10	JW33-1114A
J1	14 - 4	MS3112E22-55P
J2	14 - 5	MS3102R10SL3P
J3	14 - 69	MS3112E10-6S
J4	14 - 68	JJ089
LS1	14 - 63	25AC7Z801
PS1	14 - 47	PM23-3-750A
P1	14 - 78	JT08P16-55S
P2	14 - 78	JT08P16-55S
P3	14 - 77	JT08P12-98S
P4	14 - 77	JT08P12-98S
R41	14 - 67	383-0056-040
R42	14 - 60	57415
S1	14 - 71	MS90310-231
S2	14 - 58	259-2641-020
S3	14 - 58	259-2641-020

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S4	14 - 58	259-2641-020
S5	14 - 58	259-2641-020
S6	14 - 62	MS25068-31
S7	14 - 65	MS90311-231
S8	14 - 65	MS90311-231
TB1	14 - 38	37TB8
XA1	14 - 36	M21097-8-4
XA2	14 - 15	78S11M1005
XA3	14 - 15	78S11M1005
XA4	14 - 15	78S11M1005
XA5	14 - 15	78S11M1005
XA6	14 - 15	78S11M1005
XDS1	14 - 56	5160-458-604GRN
XDS2	14 - 55	5160-458-604WHT
XDS3	14 - 55	5160-458-604WHT
XDS4	14 - 55	5160-458-604WHT
XDS5	14 - 55	5160-458-604WHT
XDS5	14 - 55	5160-458-604WHT

CHAPTER 7

CIRCUIT DIAGRAMS

7-1. INTRODUCTION. This chapter contains all the schematic diagrams, detailed logic diagrams, and from-to wire lists required to support the principles of operation and assist in maintenance of Control-Monitor OK-145/TSC-60(V) (radio control group). The from-to wire lists are presented as tables 7-1 through 7-7. All entries in the tables are in alphanumeric order and are double-ended for quick reference. The FROM and TO columns of the wire tables indicate the connection of each wire terminating at a jack, plug, or external connector. The WIRE CODE column provides wire size and color information. That part of the wire code preceding the hyphen indicates the AWG size, and the part following the hyphen indicates the wire color, using the standard resistor color code. When only one digit follows the hyphen, a solid colored wire is indicated. If more than one digit follows the hyphen, the first digit of the color code indicates the wire body color, the second digit indicates the color of the first tracer, and the third digit indicates the color of the second tracer, etc.

Table 7-1. Receive Control Head Front Panel A8A4, Wire List

FROM	TO	WIRE CODE	FUNCTION
DS1-2	P2-17	22-9	Fault
DS3-2	P1-6	26-9	Opr
DS4-2	P1-33	▲	Prove
J1-1	P2-48	|	Dimmed 120 Vac
J1-2	P2-50	|	Dimmed 120 Vac
P1-1	S2C-12	|	Mon word 3 enable
P1-2	S1-2	|	Mon word 2 enable
P1-3	S4-2	|	Pwr change
P1-4	S10F-e	|	Freq sw change
P1-5	S11-4	|	Initiate
P1-6	DS3-2	|	Opr
P1-13	S10F-4	|	Wt-4
P1-14	S1-4	|	Pwr on
P1-15	S10F-2	|	Wt-2
P1-16	S3B-3	|	Wt-(2,4)
P1-19	S3B-7	|	Wt-2
P1-20	S10F-1	|	Wt-1
P1-21	S10D-8	|	Wt-8
P1-22	S3C-1	|	Wt-1
P1-23	S10D-4	|	Wt-4
P1-24	S7A3	|	AME enable
P1-25	S9A-2	|	B1 voice
P1-27	S10D-2	|	Wt-2
P1-29	S8A-10	▼	A1 data
P1-33	DS4-2	26-9	Prove
P1-35	S4-1	22-9	Lamp test
P1-36	S8A2	26-9	A1 voice
P1-37	S4-2	26-9	Gnd
P1-38	S10D-1	26-9	Wt-1

Table 7-1. Receive Control Head Front Panel A8A4, Wire List (Cont)

FROM	TO	WIRE CODE	FUNCTION
P2-2	S10A-L1	26-9	Bit 0
P2-3	S10E-8	▲	Wt-8
P2-4	S10A-2	|	Wt-2
P2-5	S2B-1	|	Wt-8
P2-6	S3C-12	|	Rcvr slave ident
P2-7	S10E-4	|	Wt-4
P2-8	S10A-1	|	Wt-1
P2-9	S2B-5	|	Wt-4
P2-10	S2B-3	|	Wt-2, 4
P2-11	S2B-7	|	Wt-2
P2-12	S10E-2	|	Wt-2
P2-13	S2C-1	▼	Wt-1
P2-16	S10E-1	26-9	Wt-1
P2-17	DS1-2	22-9	Fault
P2-18	S10F-8	26-9	Wt-8
P2-19	S11-3	▲	Freq initiate
P2-20	S10B-2	|	Wt-2
P2-21	S3B-1	|	Wt-8
P2-22	S10B-1	|	Wt-1
P2-23	S3B-5	|	Wt-4
P2-24	S10B-8	|	Wt-8
P2-25	S10B-4	|	Wt-4
P2-26	S10C-1	|	Wt-1
P2-27	S6A-2	|	B2 voice
P2-29	S5A-10	|	A2 data
P2-30	S6A-10	|	B2 data
P2-32	S5A-2	|	A2 voice
P2-34	S10C-2	|	Wt-2
P2-35	S9A-10	|	B1 data
P2-36	S10C-4	|	Wt-4
P2-37	S7A-8	|	Self-test enable
P2-38	S10C-8	|	Wt-8
P2-45	R1-3	▼	Lamp bus
P2-46	S8B-1	26-9	Mode initiate
P2-47	R1-2	22-9	+4.7 Vdc
P2-48	J1-1	26-9	Dimmed 120 Vac
P2-49	J10A-C	26-9	Mon word 1 enable
P2-50	J1-2	26-9	Dimmed 120 Vac
R1-2	P2-47	22-9	+4.7 Vac
R1-3	P2-45	26-9	Lamp bus
S1-2	P1-2	▲	Mon word 2 enable
S1-4	P1-14	|	Pwr on
S2B-1	P2-5	|	Wt-8
S2B-3	P2-10	|	Wt-2, 4
S2B-5	P2-9	|	Wt-4
S2B-7	P2-11	|	Wt-2
S2C-1	P2-13	▼	Wt-1
S2C-12	P1-1	26-9	Mon word 3 enable

Table 7-1. Receive Control Head Front Panel A8A4, Wire List (Cont)

FROM	TO	WIRE CODE	FUNCTION
S3B-1	P2-21	26-9	Wt-8
S3B-3	P1-16	▲	Wt-2, 4
S3B-5	P2-23	|	Wt-4
S3B-7	P1-19	|	Wt-2
S3C-1	P1-22	▼	Wt-1
S3C-12	P2-6	26-9	Rcvr slave ident
S4-1	P1-35	22-9	Lamp test
S4-2	P1-3	26-9	Pwr change
S5A-2	P2-32	▲	A2 voice
S5A-10	P2-29	|	A2 data
S6A-2	P2-27	|	B2 voice
S6A-10	P2-30	|	B2 data
S7A-3	P1-24	|	Am enable
S7A-8	P2-37	|	Self-test enable
S8A-2	P1-36	|	A1 voice
S8A-10	P1-29	|	A1 data
S8B-1	P2-46	|	Mode initiate
S9A-2	P1-25	|	B1 voice
S9A-10	P2-35	|	B1 data
S10A-1	P2-8	|	Wt-1
S10A-2	P2-4	|	Wt-2
S10A-C	P2-49	|	Mon word 1 enable
S10A-L1	P2-2	|	Bit 0
S10B-1	P2-22	|	Wt-1
S10B-2	P2-20	|	Wt-2
S10B-4	P2-25	|	Wt-4
S10B-8	P2-24	|	Wt-8
S10C-1	P2-26	|	Wt-1
S10C-2	P2-34	|	Wt-2
S10C-4	P2-36	|	Wt-4
S10C-8	P2-38	|	Wt-8
S10D-1	P1-38	|	Wt-1
S10D-2	P1-27	|	Wt-2
S10D-4	P1-23	|	Wt-4
S10D-8	P1-21	|	Wt-8
S10E-1	P2-16	|	Wt-1
S10E-2	P2-12	|	Wt-2
S10E-4	P2-7	|	Wt-4
S10E-8	P2-3	|	Wt-8
S10F-1	P1-20	|	Wt-1
S10F-2	P1-15	|	Wt-2
S10F-4	P1-13	|	Wt-4
S10F-8	P2-18	|	Wt-8
S10F-T	P1-4	|	Freq sw change
S11-3	P2-19	|	Freq initiate
S11-4	P1-5	▼	Initiate (indicator)
S4-2	P1-37	26-9	Gnd

Table 7-2. Receive Control Head Rear Panel, Wire List

FROM	TO	WIRE CODE	FUNCTION
E-1	J1-9	26-9	Gnd
E-1	J1-43	26-9	Gnd
E-1	J1-21	26-9	LL mon shld
E-1	J1-38	26-9	Gnd
E-1	P1-3	22-9	Gnd
E-1	J1-40	26-9	Gnd
E-1	J3-4	▲	Gnd
E-1	J1-15	‖	LL carrier shld
E-1	J1-46	‖	Gnd
E-1	J1-12	‖	LL DELIM shld
E-1	J1-18	‖	LL cont shld
E-1	J1-3	‖	Gnd
E-1	J1-6	▼	Gnd
E-1	J1-39	26-9	Gnd
E-1	P1-67	22-9	Gnd
J1-1	P1-55	26-9	Carrier bus
J1-2	P1-57	▲	$\overline{\text{Carrier bus}}$
J1-3	E-1	‖	Gnd
J1-4	P1-51	‖	Cont bus
J1-5	P1-49	‖	$\overline{\text{Cont bus}}$
J1-6	E-1	‖	Gnd
J1-7	P1-65	‖	Mon bus
J1-8	P1-63	▼	$\overline{\text{Mon bus}}$
J1-9	E-1	26-9	Gnd
J1-10	P1-29	22-9	Sync (LL DELIM)
J1-11	P1-20	26-9	Sync ($\overline{\text{LL DELIM}}$)
J1-12	E-1	▲	Gnd
J1-13	P1-37	‖	LL clock
J1-14	P1-36	‖	$\overline{\text{LL clock}}$
J1-15	E-1	‖	Gnd
J1-16	P1-41	‖	LL cont bus
J1-17	P1-39	‖	$\overline{\text{LL cont bus}}$
J1-18	E-1	‖	Gnd
J1-19	P1-47	‖	LL mon bus
J1-20	P1-45	‖	LL mon bus
J1-21	E-1	‖	Gnd
J1-22	P1-43	‖	Key
J1-23	P1-33	‖	VOX
J1-24	P1-30	‖	Simplex
J1-25	P1-27	‖	Rcvr thru cplr
J1-27	P1-35	‖	Servo
J1-34	P1-58	‖	A1 rcv ind
J1-35	P1-52	‖	A2 rcv ind
J1-36	P1-53	‖	B1 rcv ind
J1-37	P1-50	‖	Keyed/B2 rcv ind
J1-38	E-1	‖	Gnd
J1-39	E-1	‖	Gnd
J1-40	E-1	▼	Gnd
J1-41	P1-28	26-9	Lamp bus

Table 7-2. Receive Control Head Rear Panel, Wire List (Cont)

FROM	TO	WIRE CODE	FUNCTION
J1-42	P1-56	26-9	Lamp test 2
J1-43	E-1		Gnd
J1-44	P1-54		Lamp test 1
J1-45	PS1-9		+4.7 Vdc
J1-46	E-1		Gnd
J1-47	P1-72		Group 1
J1-48	P1-66		Group 2
J1-49	P1-70		Group 3
J1-50	P1-68		Group 4
J1-51	P1-31	26-9	Rcvr mute
J2-A	PS1-1	22-9	120 Vac
J2-B	PS1-2		120 Vac
J2-C	LUG-1		Chassis gnd
J2-D	P1-21		Dimmed 120 Vac
J2-E	P1-22		Dimmed 120 Vac
J2-F	PS1-9		+4.7 Vdc
J2-G	P1-32	22-9	+4.7 Vdc
J3-1	P1-42	26-9	Strap 2
J3-2	P1-38		Strap 1 (gnd)
J3-3	P1-40		Ext strap 3 (gnd)
J3-4	E-1		Gnd
J3-5	P1-59		Cont strap 1
J3-6	P1-61		Cont strap 2
J3-7	P1-62		Cont strap 3
J3-8	P1-64		Cont strap 4
J3-9	P1-26		Mon word 1 enable
J3-10	P1-25		Mon word 2 enable
J3-11	P1-24		Mon word 3 enable
J3-12	P1-23		Mon strap 4
J3-13	P1-2		Adrs dcd 1
J3-14	P1-1		Adrs dcd 2
J3-15	P1-4		Adrs dcd 3
J3-16	P1-8		Adrs dcd 4
J3-17	P1-6		Adrs dcd 5
J3-18	P1-10		Adrs dcd 6
J3-19	P1-9		Adrs dcd 7
J3-20	P1-11		Adrs dcd 8
J3-21	P1-12		Adrs dcd 9
J3-22	P1-13		Adrs dcd 10
J3-23	P1-14		Adrs dcd 11
J3-24	P1-15		Adrs dcd 12
J3-25	P1-16		Adrs dcd 13
J3-26	P1-17		Adrs dcd 14
J3-27	P1-18		Adrs dcd 15
J3-28	P1-19		Adrs dcd 16
P1-1	J3-14		Adrs dcd 2
P1-2	J3-13	26-9	Adrs dcd 1
P1-3	E-1	22-9	Gnd

Table 7-2. Receive Control Head Rear Panel, Wire List (Cont)

FROM	TO	WIRE CODE	FUNCTION
P1-4	J3-15	26-9	Adrs dcd 3
P1-5	PS1-7	22-9	-26 Vdc
P1-6	J3-17	26-9	Adrs dcd 5
P1-7	PS1-5	22-9	+12 Vdc
P1-8	J3-16	26-9	Adrs dcd 4
P1-9	J3-19	▲	Adrs dcd 7
P1-10	J3-18	|	Adrs dcd 6
P1-11	J3-20	|	Adrs dcd 8
P1-12	J3-21	|	Adrs dcd 9
P1-13	J3-22	|	Adrs dcd 10
P1-14	J3-23	|	Adrs dcd 11
P1-15	J3-24	|	Adrs dcd 12
P1-16	J3-25	|	Adrs dcd 13
P1-17	J3-26	|	Adrs dcd 14
P1-18	J3-27	|	Adrs dcd 15
P1-19	J3-28	▼	Adrs dcd 16
P1-20	J1-11	26-9	Sync ($\overline{\text{LL DELIM}}$)
P1-21	J2-D	22-9	Dimmed 120 Vac
P1-22	J2-E	22-9	Dimmed 120 Vac
P1-23	J3-12	26-9	Mon strap 4
P1-24	J3-11	▲	Mon word 3 enable
P1-25	J3-10	|	Mon word 2 enable
P1-26	J3-9	|	Mon word 1 enable
P1-27	J1-25	▼	Rcvr thru cplr
P1-28	J1-41	26-9	Lamp bus
P1-29	J1-10	22-9	Sync (LL DELIM)
P1-30	J1-24	26-9	Simplex
P1-31	J1-51	26-9	Rcvr mute
P1-32	J2-G	22-9	+4.7 Vdc
P1-33	J1-23	26-9	VOX
P1-35	J1-27	▲	Servo
P1-36	J1-14	|	$\overline{\text{LL clock}}$
P1-37	J1-13	|	$\overline{\text{LL clock}}$
P1-38	J3-2	|	Strap 1 (gnd)
P1-39	J1-17	|	$\overline{\text{LL cont bus}}$
P1-40	J3-3	|	Ext strap 3 (gnd)
P1-41	J1-16	|	LL cont bus
P1-42	J3-1	|	Strap 2
P1-43	J1-22	|	Key
P1-45	J1-20	|	$\overline{\text{LL mon bus}}$
P1-47	J1-19	|	LL mon bus
P1-49	J1-5	|	$\overline{\text{Cont bus}}$
P1-50	J1-37	|	Keyed/B2 rcv ind
P1-51	J1-4	|	Cont bus
P1-52	J1-35	|	A2 rcv ind
P1-53	J1-36	|	B1 rcv ind
P1-54	J1-44	|	Lamp test 1
P1-55	J1-1	▼	Carrier bus

Table 7-2. Receive Control Head Rear Panel, Wire List (Cont)

FROM	TO	WIRE CODE	FUNCTION
P1-56	J1-42	26-9	Lamp test 2
P1-57	J1-2	▲	$\overline{\text{Carrier bus}}$
P1-58	J1-34		A1 rcv ind
P1-59	J3-5		Cont strap 1
P1-61	J3-6		Cont strap 2
P1-62	J3-7		Cont strap 3
P1-63	J1-8		$\overline{\text{Mon bus}}$
P1-64	J3-8		Cont strap 4
P1-65	J1-7	▼	Mon bus
P1-66	J1-48	26-9	Group 2
P1-67	E-1	22-9	Gnd
P1-68	J1-50	26-9	Group 4
P1-70	J1-49	26-9	Group 3
P1-71	PS1-3	22-9	+5 Vdc
P1-72	J1-47	26-9	Group 1
PS1-1	J2-A	22-9	120 Vac A
PS1-2	J2-B	▲	120 Vac B
PS1-3	P1-71		+5 Vdc
PS1-5	P1-7		+12 Vdc
PS1-7	P1-5	▼	-26 Vdc
PS1-9	J2-F	22-9	+4.7 Vdc
PS1-9	J1-45	26-9	+4.7 Vdc

Table 7-3. Receive Control Head A8A5J3 Address Strapping, Wire List

FROM	TO	WIRE CODE	FUNCTION
A8A5J3-5	A8A5J3-15	26-9	Cont strap 1/adrs dcd 3
A8A5J3-9	A8A5J3-17	▲	Mon word 1 enbl/adrs dcd 5
A8A5J3-10	A8A5J3-25		Mon word 2 enbl/adrs dcd 13
A8A5J3-11	A8A5J3-21		Mon word 3 enbl/adrs dcd 9
A8A5J3-15	A8A5J3-5		Cont strap 1/adrs dcd 3
A8A5J3-17	A8A5J3-9		Mon word 1 enbl/adrs dcd 5
A8A5J3-21	A8A5J3-11	▼	Mon word 3 enbl/adrs dcd 9
A8A5J3-25	A8A5J3-10	26-9	Mon word 2 enbl/adrs dcd 13

Table 7-4. Transmit Control Head Front Panel A7A9, Wire List

FROM	TO	WIRE CODE	FUNCTION
A10J1-28	S7B-5	26-9	Cw intlk A
A10J1-29	S7B-1	↑	Cw intlk B
A10J1-30	S7B-6		Cw intlk common
A10J1-31	S2-2		Key intlk A
A10J1-32	S1C-10	↓	Key intlk B
A10J1-33	S2-4	26-9	VOX intlk A
DS1-2	P2-17	22-9	Fault
DS2-2	P1-37	↑	Gnd
DS3-2	P1-6		Opr
DS4-2	P1-33		Prove
DS5-2	P1-31		Key
J1-1	P2-48	↓	Dimmed 120 Vac
J1-2	P2-50	22-9	Dimmed 120 Vac
J2-2	S4-1	26-9	Bit 0
P1-1	S3A-12	↑	Mon word 3 enable
P1-2	S7A-6		Mon word 2 enable
P1-3	S1B-1	↓	Pwr change
P1-4	S10F-C1	26-9	Freq switch change
P1-5	S11-4	22-9	Initiate (indicator)
P1-6	DS3-2	22-9	Opr
P1-13	S10F-4	26-9	Wt-4
P1-14	S1A-2	↑	Fil enable
P1-15	S10F-2		Wt-2
P1-17	S1C-3		Plate enable
P1-18	S3B-1		Wt-8
P1-20	S10F-1		Wt-1
P1-21	S10D-8		Wt-8
P1-23	S10D-4		Wt-4
P1-24	S7A-3		AME enable
P1-26	S3B-7		Wt-4
P1-27	S10D-2		Wt-2
P1-29	S5-2	↓	A2 xmt
P1-30	S3B-9	26-9	Wt-2
P1-31	DS5-2	22-9	Key
P1-32	S3B-5	26-9	Wt-(2, 4)
P1-33	DS5-2	22-9	Prove
P1-34	S3A-3	26-9	Wt-1
P1-35	S4-2	26-9	Lamp test
P1-37	DS2-2	22-9	Gnd
P1-38	S10D-1	26-9	Wt-1
P2-1	S4-1	↑	Master/slave
P2-3	S10E-8		Wt-8
P2-4	S10A-2		Wt-2
P2-7	S10E-4		Wt-4
P2-8	S10A-1		Wt-1
P2-12	S10E-2		Wt-2
P2-15	S1A-10	↓	Low pwr
P2-16	S10E-1	26-9	Wt-1

Table 7-4. Transmit Control Head Front Panel A7A9, Wire List (Cont)

FROM	TO	WIRE CODE	FUNCTION
P2-17	DS1-2	22-9	Fault
P2-18	S10F-8	26-9	Wt-8
P2-19	S11-3	↑	Freq initiate
P2-20	S10B-2		Wt-2
P2-22	S10B-1		Wt-1
P2-24	S10B-8		Wt-8
P2-25	S10B-4		Wt-4
P2-26	S10C-1		Wt-1
P2-28	S7A-4		Cw enable
P2-29	S8-2		A1 xmt
P2-30	S9-2		B1 xmt
P2-33	S2-6		Key
P2-34	S10C-2		Wt-2
P2-35	S6-2		B2 xmt
P2-36	S10C-4		Wt-4
P2-37	S7A-2	↓	Self-test enable
P2-38	S10C-8	26-9	Wt-8
P2-45	R1-3	22-9	Lamp bus
P2-46	S8-7	26-9	Mode initiate
P2-47	R1-2	22-9	+4.7 Vdc
P2-48	J1-1	22-9	Dimmed 120 Vac
P2-49	S10F-C	26-9	Mon word enable
P2-50	J1-2	22-9	Dimmed 120 Vac
R1-2	P2-47	22-9	+4.7 Vdc
R1-3	P2-45	22-9	Lamp bus
S1A-2	P1-14	26-9	Fil enable
S1A-10	P2-15	↑	Low pwr
S1B-1	P1-3		Pwr change
S1C-3	P1-17		Plate enable
S1C-10	A10J1-32		Key intlk B
S2-2	A10J1-31		Key intlk A
S2-4	A10J1-33		VOX intlk
S2-6	P2-33		Key
S3A-3	P1-34		Wt-1
S3A-12	P1-1		Mon word 3 enable
S3B-1	P1-18		Wt-8
S3B-5	P1-32		Wt-(2, 4)
S3B-7	P1-26		Wt-4
S3B-9	P1-30		Wt-2
S4-1	P2-1		Master/slave
S4-1	J2-2		Bit 0
S4-2	P1-35		Lamp test
S5-2	P1-29		A2 xmt
S6-2	P2-35		B2 xmt
S7A-2	P2-37		Self-test enable
S7A-3	P1-24		AME enable
S7A-4	P2-28		Cw enable
S7A-6	P1-2	26-9	Mon word 2 enable

Table 7-4. Transmit Control Head Front Panel A7A9, Wire List (Cont)

FROM	TO	WIRE CODE	FUNCTION
S7B-1	A10J1-29	26-9	Cw intlk B
S7B-5	A10J1-28		Cw intlk A
S7B-6	A10J1-30		Cw intlk common
S8-2	P2-29		A1 xmit
S8-7	P2-46		Mode initiate
S9-2	P2-30		B1 xmt
S10A-1	P2-8		Wt-1
S10A-2	P2-4		Wt-2
S10B-1	P2-22		Wt-1
S10B-2	P2-20		Wt-2
S10B-4	P2-25		Wt-4
S10B-8	P2-24		Wt-8
S10C-1	P2-26		Wt-1
S10C-2	P2-34		Wt-2
S10C-4	P2-36		Wt-4
S10C-8	P2-38		Wt-8
S10D-1	P1-38		Wt-1
S10D-2	P1-27		Wt-2
S10D-4	P1-23		Wt-4
S10D-8	P1-21		Wt-8
S10E-1	P2-16		Wt-1
S10E-2	P2-12		Wt-2
S10E-4	P2-7		Wt-4
S10E-8	P2-3		Wt-8
S10F-C	P2-49		Mon word enable
S10-C1	P1-4		Freq switch change
S10F-1	P1-20		Wt-1
S10F-2	P1-15		Wt-2
S10F-4	P1-13		Wt-4
S10F-8	P2-18		Wt-8
S11-3	P2-19		Freq initiate
S11-4	P1-5	26-9	Initiate (indicator)

Table 7-5. Transmit Control Head Rear Panel, Wire List

FROM	TO	WIRE CODE	FUNCTION
E-1	J1-21	26-9	LL mon shld
E-1	J1-18	26-9	LL cont shld
E-1	P1-3	26-9	Gnd
E-1	J1-12	26-9	LL DELM shld
No Connection	J1-3	26-9	
No Connection	J1-6	26-9	
No Connection	J1-9	26-9	

Table 7-5. Transmit Control Head Rear Panel, Wire List (Cont)

FROM	TO	WIRE CODE	FUNCTION
E-1	J1-15	26-9	LL carrier shld
E-1	J1-43		Gnd
E-1	J1-39		Gnd
E-1	J3-4		Gnd
E-1	J1-38		Gnd
E-1	J1-40		Gnd
E-1	J1-46	26-9	Gnd
E-1	P1-67	22-9	Gnd
E-2	J2-C	22-9	Chassis gnd
J1-1	P1-55	18-bus	Carrier bus
J1-2	P1-57	26-9	Carrier bus
J1--3	No Connection		
J1-4	P1-51		Cont bus
J1-5	P1-49		Cont bus
J1-6	No Connection		
J1-7	P1-65		
J1-8	P1-63		Mon bus
J1-9	No Connection		Mon bus
J1-10	P1-29		Sync (LL DELIM)
J1-11	P1-20		Sync (LL DELIM)
J1-12	E-1		Gnd
J1-13	P1-37		LL clock
J1-14	P1-36		LL clock
J1-15	E-1		Gnd
J1-16	P1-41		LL cont bus
J1-17	P1-39		LL cont bus
J1-18	E-1		Gnd
J1-19	P1-47		LL mon bus
J1-20	P1-45		LL mon bus
J1-21	E-1		Gnd
J1-22	P1-43		Key
J1-23	P1-33		VOX
J1-24	P1-30		Simplex
J1-25	P1-27		Rcvr thru cplr
J1-26	P1-46		Front pnl key
J1-27	P1-35		Servo
J1-28	S7B-5		Cw intlk A
J1-29	S7B-1		Cw intlk B
J1-30	S7B-6		Cw intlk C
J1-31	S2-2		Key intlk A
J1-32	S1C-10		Key intlk B
J1-33	S2-4		VOX intlk
J1-34	P1-50		Keyed/B2 rcv ind
J1-35	P1-52		A2 rcv ind
J1-36	P1-53		B1 rcv ind
J1-37	P1-58		A1 rcv ind
J1-38	E-1		Gnd
J1-39	E-1	26-9	Gnd

Table 7-5. Transmit Control Head Rear Panel, Wire List (Cont)

FROM	TO	WIRE CODE	FUNCTION
J1-40	E-1	26-9	Gnd
J1-41	P1-28		Lamp bus
J1-42	P1-56		Lamp test 2
J1-43	E-1		Gnd
J1-44	P1-54		Lamp test 1
J1-45	PS1-9		+4.7 Vdc
J1-46	E-1		Gnd
J1-47	P1-72		+4.7 Vdc
J1-48	P1-66		Group 2
J1-49	P1-70		Group 3
J1-50	P1-68		Group 4
J1-51	P1-31	26-9	Rcvr mute
J2-A	PS1-1	22-9	120 VAC
J2-B	PS1-2		120 VAC
J2-C	E-2		Gnd
J2-D	P1-21		Dimmed 120 Vac
J2-E	P1-22		Dimmed 120 Vac
J2-F	PS1-9		+4.7 Vdc
J2-G	P1-32	22-9	+4.7 Vdc
J3-1	P1-42	26-9	Strap 2
J3-2	P1-38		Strap 1 (gnd)
J3-3	P1-40		Ext Strap 3 (gnd)
J3-4	E-1		Gnd
J3-5	P1-59		Cont strap 1
J3-6	P1-61		Cont strap 2
J3-7	P1-62		Cont strap 3
J3-8	P1-64		Mon word 1 enable
J3-10	P1-25		Mon word 2 enable
J3-11	S1-2		Mon word 3 enable
J3-12	P1-23		Mon strap 4
J3-13	P1-2		Adrs dcd 1
J3-14	P1-1		Adrs dcd 2
J3-15	P1-4		Adrs dcd 3
J3-16	P1-8		Adrs dcd 4
J3-17	P1-6		Adrs dcd 5
J3-18	P1-10		Adrs dcd 6
J3-19	P1-9		Adrs dcd 7
J3-20	P1-11		Adrs dcd 8
J3-21	P1-12		Adrs dcd 9
J3-23	P1-14		Adrs dcd 11
J3-24	P1-15		Adrs dcd 12
J3-25	P1-16		Adrs dcd 13
J3-26	P1-17		Adrs dcd 14
J3-27	P1-18		Adrs dcd 15
J3-28	P1-19		Adrs dcd 16
P1-1	J3-14		Adrs dcd 2
P1-2	J3-13		Adrs dcd 1
P1-3	E-1		Gnd
P1-4	J3-15	26-9	Adrs dcd 3

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Table 7-5. Transmit Control Head Rear Panel, Wire List (Cont)

FROM	TO	WIRE CODE	FUNCTION
P1-5	PS1-7	22-9	-26 Vdc
P1-6	J3-17	26-9	Adrs dcd 5
P1-7	PS1-5	22-9	+12 Vdc
P1-8	J3-16	26-9	Adrs dcd 4
P1-9	J3-19	▲	Adrs dcd 7
P1-10	J3-18	▲	Adrs dcd 6
P1-11	J3-20	▲	Adrs dcd 8
P1-12	J3-21	▲	Adrs dcd 9
P1-13	J3-22	▲	Adrs dcd 10
P1-14	J3-23	▲	Adrs dcd 11
P1-15	J3-24	▲	Adrs dcd 12
P1-16	J3-25	▲	Adrs dcd 13
P1-17	J3-26	▲	Adrs dcd 14
P1-18	J3-27	▲	Adrs dcd 15
P1-19	J3-28	▼	Adrs dcd 16
P1-20	J1-11	26-9	$\overline{\text{Sync}}$ ($\overline{\text{LL DELIM}}$)
P1-21	J2-D	22-9	Dimmed 120 Vac
P1-22	J2-E	22-9	Dimmed 120 Vac
P1-23	J3-12	26-9	Mon strap 4
P1-24	S1-2	22-9	Mon word 3 enable
P1-25	J3-10	26-9	Mon word 2 enable
P1-26	J3-9	▲	Mon word 1 enable
P1-27	J1-25	▲	Rcvr thru cplr
P1-28	J1-41	▲	Lamp bus
P1-29	J1-10	▲	Sync (LL DELIM)
P1-30	J1-24	▼	Simplex
P1-31	J1-51	26-9	Rcvr mute
P1-32	J2-G	22-9	+4.7 Vdc
P1-33	J1-23	26-9	VOX
P1-35	J1-27	▲	Servo
P1-36	J1-14	▲	$\overline{\text{LL clock}}$
P1-37	J1-13	▲	LL clock
P1-38	J3-2	▲	Strap 1 (gnd)
P1-39	J1-17	▲	$\overline{\text{LL cont bus}}$
P1-40	J3-3	▲	Ext strap 3 (gnd)
P1-41	J1-16	▲	LL cont bus
P1-42	J3-1	▼	Strap 2
P1-43	J1-22	26-9	Key
P1-44	S1-1	22-9	548 U enable
P1-45	J1-20	26-9	$\overline{\text{LL mon bus}}$
P1-46	J1-26	▲	Front pnl key
P1-47	J1-19	▲	LL mon bus
P1-49	J1-5	▲	$\overline{\text{Cont bus}}$
P1-50	J1-34	▲	Keyed/B2 rcv ind
P1-51	J1-4	▲	Cont bus
P1-52	J1-35	▲	A2 rcv ind
P1-53	J1-36	▼	B1 rcv ind
P1-54	J1-44	26-9	Lamp test 1

Table 7-5. Transmit Control Head Rear Panel, Wire List (Cont)

FROM	TO	WIRE CODE	FUNCTION
P1-55	J1-1	18 GA bus	Carrier bus
P1-56	J1-42	26-9	Lamp test 2
P1-57	J1-2		$\overline{\text{Carrier bus}}$
P1-58	J1-37		A1 rcv ind
P1-59	J3-5		Cont strap 1
P1-61	J3-6		Cont strap 2
P1-62	J3-7		Cont strap 3
P1-63	J1-8		$\overline{\text{Mon bus}}$
P1-64	J3-8		Cont strap 4
P1-65	J1-7		Mon bus
P1-66	J1-48		Group 2
P1-67	E-1		Gnd
P1-68	J1-50		Group 4
P1-70	J1-49	26-9	Group 3
P1-71	PS1-3	22-9	+5 Vdc
P1-72	J1-47	26-9	Group 1
PS1-1	J2-A	22-9	120 Vac
PS1-2	J2-B		120 Vac
PS1-3	P1-71		+5 Vdc
PS1-4	E-1		Gnd
PS1-5	P1-7		+12 Vdc
PS1-6	E-1		Gnd
PS1-7	P1-5		-26 Vdc
PS1-8	E-1		Gnd
PS1-9	J2-F	22-9	+4.7 Vdc
PS1-9	J1-45	26-9	+4.7 Vdc
S1-1	P1-44	26-9	548U enable
S1-2	P1-24	22-9	Mon word 3 enable
S1-2	J3-11	26-9	Mon strap 3

Table 7-6. Transmit Control Head A7A10J3 Address Strapping, Wire List

FROM	TO	WIRE CODE	FUNCTION
A7A10J3-3	A7A10J3-4	26-9	Gnd
A7A10J3-4	A7A10J3-3		Gnd
A7A10J3-5	A7A10J3-14		Cont strap 1/adrs dcd 2
A7A10J3-9	A7A10J3-19		Mon word 2 enbl/adrs dcd 7
A7A10J3-10	A7A10J3-27		Mon word 1 enbl/adrs dcd 15
A7A10J3-11	A7A10J3-23		Mon word 3 enbl/adrs dcd 11
A7A10J3-14	A7A10J3-5		Cont strap 1/adrs dcd 2
A7A10J3-19	A7A10J3-9		Mon word 2 enbl/adrs dcd 7
A7A10J3-23	A7A10J3-11		Mon word 3 enbl/adrs dcd 11
A7A10J3-27	A7A10J3-10	26-9	Mon word 1 enbl/adrs dcd 15

Table 7-7. Audio Control Unit, Wire List

FROM	TO	WIRE CODE	FUNCTION
E-1	J1-A	26-0	Gnd
FL1-1	J2-A	20-98	120 Vac
FL2-1	J2-B	20-98	120 Vac, neutral
FL3-1	J1-3	26-92	Carrier (clock)
FL3-2	P1-1	26-92	$\overline{\text{Carrier (clock)}}$
FL3-3	J1-AA	26-92	Carrier (clock)
FL3-4	P1-2	26-92	$\overline{\text{Carrier (clock)}}$
FL4-1	J1-CC	26-95	Control
FL4-2	P1-4	26-95	$\overline{\text{Control}}$
FL4-3	J1-DD	26-95	Control
FL4-4	P1-5	26-95	$\overline{\text{Control}}$
FL5-1	J1-FF	26-96	Monitor
FL5-2	P1-7	26-96	$\overline{\text{Monitor}}$
FL5-3	J1-GG	26-96	Monitor
FL5-4	P1-8	26-96	$\overline{\text{Monitor}}$
J1-A	E1	26-0	Gnd
J1-AA	FL3-3	26-92	Carrier (clock)
J1-a	XA1-31	26-9095	B2 receive
J1-B	XA6-3	26-92	Test point
J1-BB	Open	26-92	Shld
J1-b	XA1-83	26-9095	B2 receive
J1-C	XA6-4	26-92	Test point
J1-CC	FL4-1	26-95	Control
J1-c	XA3-1	26-92	Mike
J1-D	XA5-3	26-92	Test point
J1-DD	FL4-3	26-95	Control
J1-d	XA3-2	26-92	Test point
J1-E	XA5-04	26-92	Test point
J1-EE	Open	26-95	Shld
J1-e	XA2-1	26-92	Test point
J1-F	S6-9	26-92	Order wire
J1-FF	FL5-1	26-96	Monitor
J1-f	XA2-2	26-92	Test point
J1-G	S6-12	26-92	Order wire
J1-GG	FL5-3	26-96	$\overline{\text{Monitor}}$
J1-g	XA5-1	26-92	Test point
J1-H	XA1-11	26-92	Monitor bus
J1-HH	Open	26-96	Shld
J1-h	XA5-2	26-92	Test point
J1-J	XA1-10	26-92	Monitor bus
J1-j	XA2-4	26-92	Test point
J1-K	S2A-11	26-93	A2 transmit
J1-k	XA2-3	26-92	A2 transmit
J1-L	S2B-3	26-93	A2 transmit
J1-M	S3A-11	26-95	A1 transmit
J1-N	S3B-3	26-95	A1 transmit
J1-P	S4A-11	26-9093	B1 transmit
J1-R	S4B-3	26-9093	B1 transmit

Table 7-7. Audio Control Unit, Wire List (Cont)

FROM	TO	WIRE CODE	FUNCTION
J1-S	S5A-11	26-9095	B2 transmit
J1-T	S5B-3	26-9095	B2 transmit
J1-U	XA1-44	26-93	A2 receive
J1-V	XA1-86	26-93	A2 receive
J1-W	XA1-39	26-95	A1 receive
J1-X	XA1-85	26-95	A1 receive
J1-y	S8-3	26-1	Ptt key
J1-Y	XA1-35	26-9093	B1 receive
J1-x	P1-32	26-0	Ptt key
J1-Z	XA1-84	26-9093	B1 receive
J1-z	FL3-1	26-92	Carrier (clock)
J2-A	FL1-1	20-98	120 Vac
J2-B	FL2-1	20-98	120 Vac, neutral
J2-C	TB1-5	26-0	Gnd
J3-A	XA4-1	26-906	Microphone
J3-B	XA4-2	26-906	Microphone
J3-C	S7-3	26-92	Earphone
J3-D	S7-6	26-92	Earphone
J3-E	P1-29	26-1	Ptt switch input
J3-F	J4-TIP	26-1	Ptt switch input
J4-Sleeve	P1-28	26-6	Cw intlk A
J4-Tip	J3-F	26-1	Ptt
J4-Tip	S8-2	26-1	VOX
Open	P1-3	26-92	Shld
Open	P1-9	26-96	Shld
Open	J1-BB	26-92	Shld
Open	P1-6	26-95	Shld
Open	J1-EE	26-95	Shld
Open	J1-HH	26-96	Shld
P1-1	FL3-2	26-92	Carrier (clock)
P1-2	FL3-4	26-92	Carrier (clock)
P1-3	Open	26-92	Shld
P1-4	FL4-2	26-95	Control
P1-5	FL4-4	26-95	Control
P1-6	Open	26-95	Shld
P1-7	FL5-2	26-96	Monitor
P1-8	FL5-4	26-96	Monitor
P1-9	Open	26-96	Shld
P1-10	P2-10	26-9092	Delimiter bus
P1-11	P2-11	26-9092	Delimiter bus
P1-12	P2-12	26-9092	Shld
P1-13	P2-13	26-903	Clock bus
P1-14	P2-14	26-903	Clock bus
P1-15	P2-15	26-903	Shld
P1-16	P2-16	26-905	Control bus
P1-17	P2-17	26-905	Control bus
P1-18	P2-18	26-905	Shld
P1-19	P2-19	26-906	Monitor
P1-20	P2-20	26-906	Monitor bus

Table 7-7. Audio Control Unit, Wire List (Cont)

FROM	TO	WIRE CODE	FUNCTION
P1-21	P2-21	26-906	Shld
P1-22	P1-26	26-1	Key strap
P1-23	S8-5	26-3	VOX entry
P1-24	S1-2	26-4	Simplex entry
P1-25	S1-1	26-9	Rcvr thru coupler
P1-26	P1-22	26-1	Key strap
P1-28	J4-sleeve	26-6	Cw intlk A
P1-29	J3-E	26-1	Ptt
P1-30	P1-31	26-0	Cw interlock common
P1-31	P1-30	26-0	Key interlock A
P1-32	J1-x	26-0	Key interlock B
P1-33	S8-4	26-5	VOX intlk
P1-38	S1-1	26-0	Gnd
P1-39	P2-39	26-0	Gnd
P1-40	XDS1-1	26-0	Gnd
P1-42	P1-44	26-1	Lamp test strap
P1-43	P1-48	26-1	Gnd
P1-44	P1-42	26-1	Lamp test strap
P1-48	P1-43	26-1	Radio group 2
P2-10	P1-10	26-9092	Delimiter bus
P2-11	P1-11	26-9092	Delimiter bus
P2-12	P1-12	26-9092	Delimiter bus shld
P2-13	P1-13	26-903	Clock bus
P2-14	P1-14	26-903	Clock bus
P2-15	P1-15	26-903	Clock bus shld
P2-16	P1-16	26-905	Control bus
P2-17	P1-17	26-905	Control bus
P2-18	P1-18	26-905	Control bus shld
P2-19	P1-19	26-906	Monitor bus
P2-20	P1-20	26-906	Monitor bus
P2-21	P1-21	26-906	Monitor bus shld
P2-34	XDS3-1	26-3	Receive indicator A1
P2-35	XDS2-1	26-4	Receive indicator A2
P2-36	XDS4-1	26-5	Receive indicator B1
P2-37	XDS5-1	26-6	Receive indicator B2
P2-38	S1-1	26-0	Gnd
P2-39	P1-39	26-0	Gnd
P2-40	XDS1-1	26-0	Gnd
P2-41	XDS2-2	26-0	Lamp test strap
P2-42	P2-44	26-1	Gnd
P2-43	P2-48	--	Gnd
P2-44	P2-42	26-1	Lamp test strap
P2-48	P4-43	--	Radio group 2
P3-A	TB1-11	20-98	120 Vac
P3-B	TB1-12	20-98	120 Vac
P3-C	TB1-13	22-0	Gnd
P3-D	TB1-15	20-88	Dimmed 120 Vac
P3-E	TB1-16	20-88	Dimmed 120 Vac
P3-F	P3-G	26-0	Blackout strap

Table 7-7. Audio Control Unit, Wire List (Cont)

FROM	TO	WIRE CODE	FUNCTION
P3-G	P3-F	22-0	Blackout strap
P4-A	TB1-11	20-98	120 Vac
P4-B	TB1-12	20-98	120 Vac
P4-C	TB1-13	22-0	Gnd
P4-D	TB1-15	20-88	Dimmed 120 Vac
P4-E	TB1-16	20-88	Dimmed 120 Vac
P4-F	P4-G	22-0	Blackout strap
P4-G	P4-F	22-0	Blackout strap
S1-1	P1-25	26-9	Rcvr thru coupler
S1-1	P1-38	26-0	Gnd
S1-1	P2-38	26-0	Gnd
S1-2	P1-24	26-4	Simplex entry
S2A-11	J1-K	26-93	A2 transmit
S2B-3	J1-L	26-93	A2 transmit
S3A-11	J1-M	26-95	A1 transmit
S3B-3	J1-N	26-95	A1 transmit
S4A-11	J1-P	26-9093	B1 transmit
S4B-3	J1-R	26-9093	B1 transmit
S5A-11	J1-S	26-9095	B2 transmit
S5B-3	J1-T	26-9095	B2 transmit
S7-6	J3-D	26-92	Earphone
S8-2	J4-Tip	26-1	VOX
S8-3	J1-y	26-1	Ptt key
S8-4	P1-33	26-5	VOX intlk
S8-5	P1-23	26-3	VOX entry
TB1-5	J2-C	26-0	Gnd
TB1-11	P4-A	20-98	120 Vac
TB1-11	P3-A	20-98	120 Vac
TB1-12	P3-B	20-98	120 Vac
TB1-12	P4-B	20-98	120 Vac
TB1-13	P4-C	22-0	Gnd
TB1-13	P3-C	22-0	Gnd
TB1-15	P3-D	20-88	Dimmed 120 Vac
TB1-15	P4-D	20-88	Dimmed 120 Vac
TB1-16	P4-E	20-88	Dimmed 120 Vac
TB1-16	P3-E	20-88	Dimmed 120 Vac
XA1-10	J1-J	26-92	Monitor bus
XA1-11	J1-H	26-92	Monitor bus
XA1-31	J1-a	26-9095	B2 receive
XA1-35	J1-Y	26-9093	B1 receive
XA1-39	J1-W	26-95	A1 receive
XA1-44	J1-U	26-93	A2 receive
XA1-83	J1-b	26-9095	B2 receive
XA1-84	J1-Z	26-9093	B1 receive
XA1-85	J1-X	26-95	A1 receive
XA1-86	J1-V	26-93	A2 receive
XA2-1	J1-e	26-92	Test point
XA2-2	J1-f	26-92	Test point
XA2-3	J1-k	26-92	A2 transmit

Table 7-7. Audio Control Unit, Wire List (Cont)

FROM	TO	WIRE CODE	FUNCTION
XA2-4	J1-j	26-92	Test point
XA3-1	J1-c	26-92	Mike
XA3-2	J1-d	26-92	Test point
XA4-1	J3-A	26-906	Microphone
XA4-2	J3-B	26-906	Microphone
XA5-1	J1-g	26-92	Test point
XA5-2	J1-h	26-92	Test point
XA5-3	J1-D	26-92	Test point
XA5-4	J1-E	26-92	Test point
XA6-3	J1-B	26-92	Test point
XA6-4	J1-C	26-92	Test point
XDS1-1	P1-40	26-0	Gnd
XDS1-1	P2-40	26-0	Gnd
XDS2-1	P2-35	26-4	Receive indicator A2
XDS2-2	P2-41	26-0	4.7-Vdc lamp bus
XDS3-1	P2-34	26-3	Receive indicator A1
XDS4-1	P2-36	26-5	Receive indicator B1
XDS4-1	P2-37	26-6	Receive indicator B2

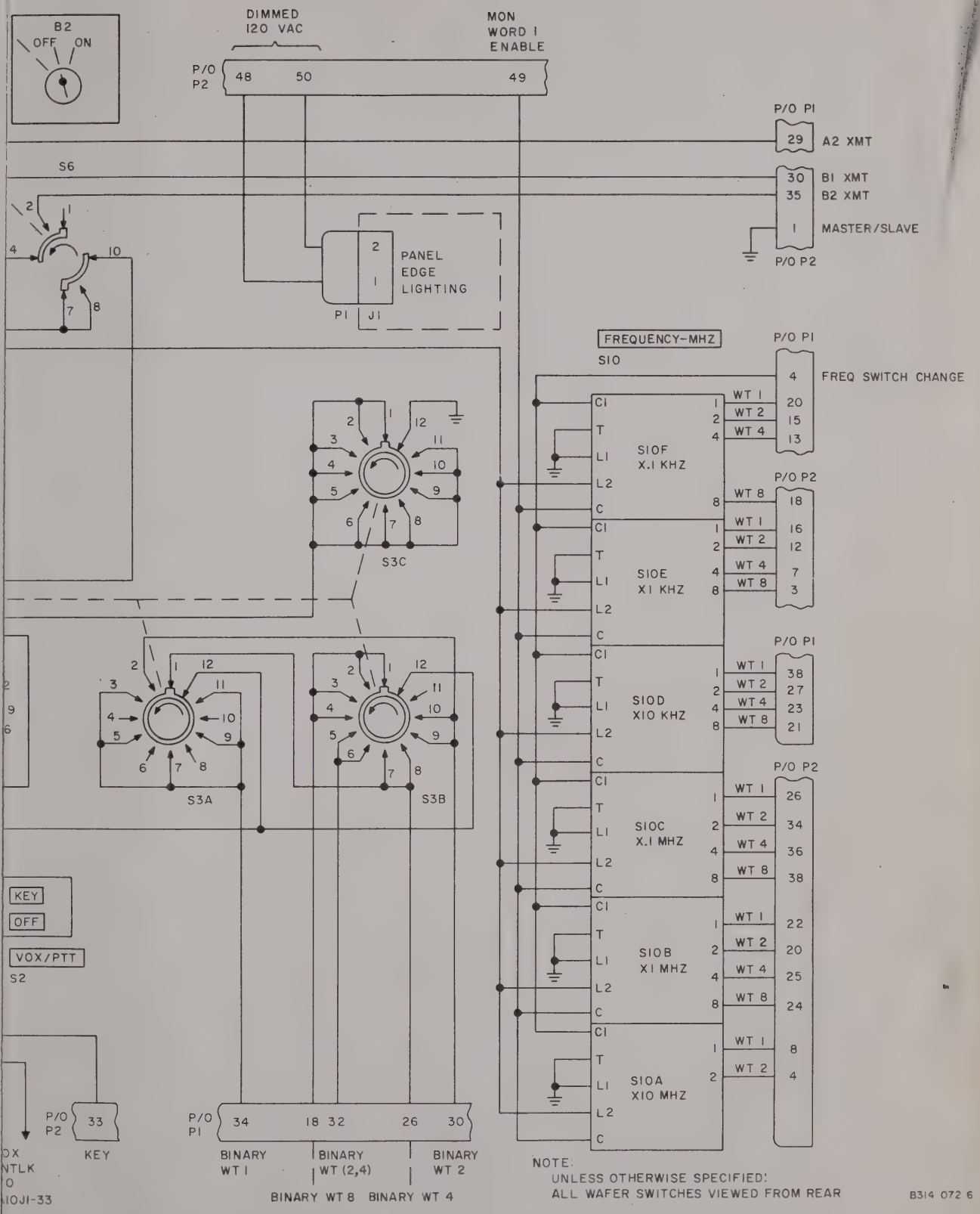


Figure 7-1. Transmit Control Head Front Panel, Schematic Diagram

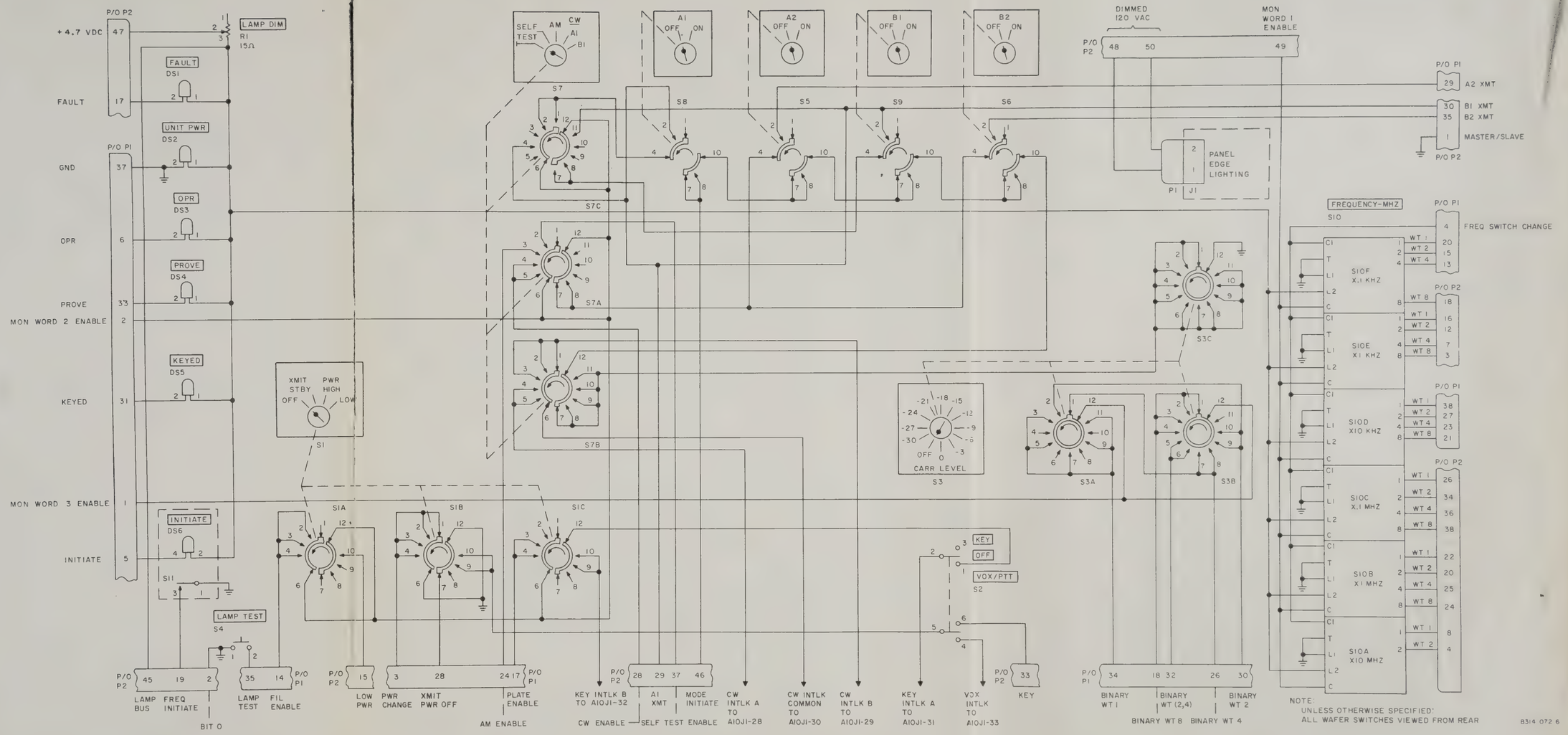


Figure 7-1. Transmit Control Head Front Panel, Schematic Diagram

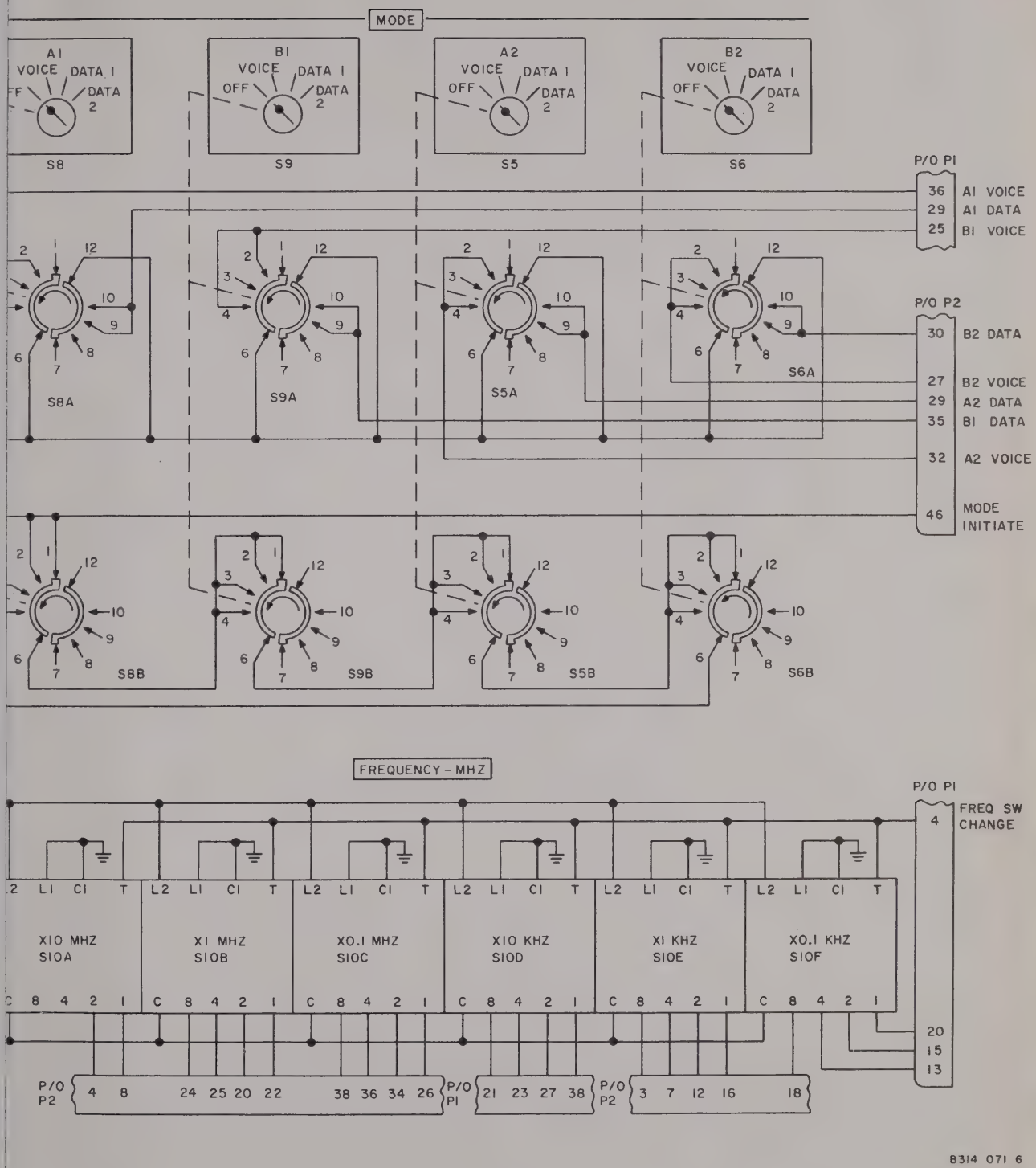


Figure 7-2. Receive Control Head Front Panel, Schematic Diagram

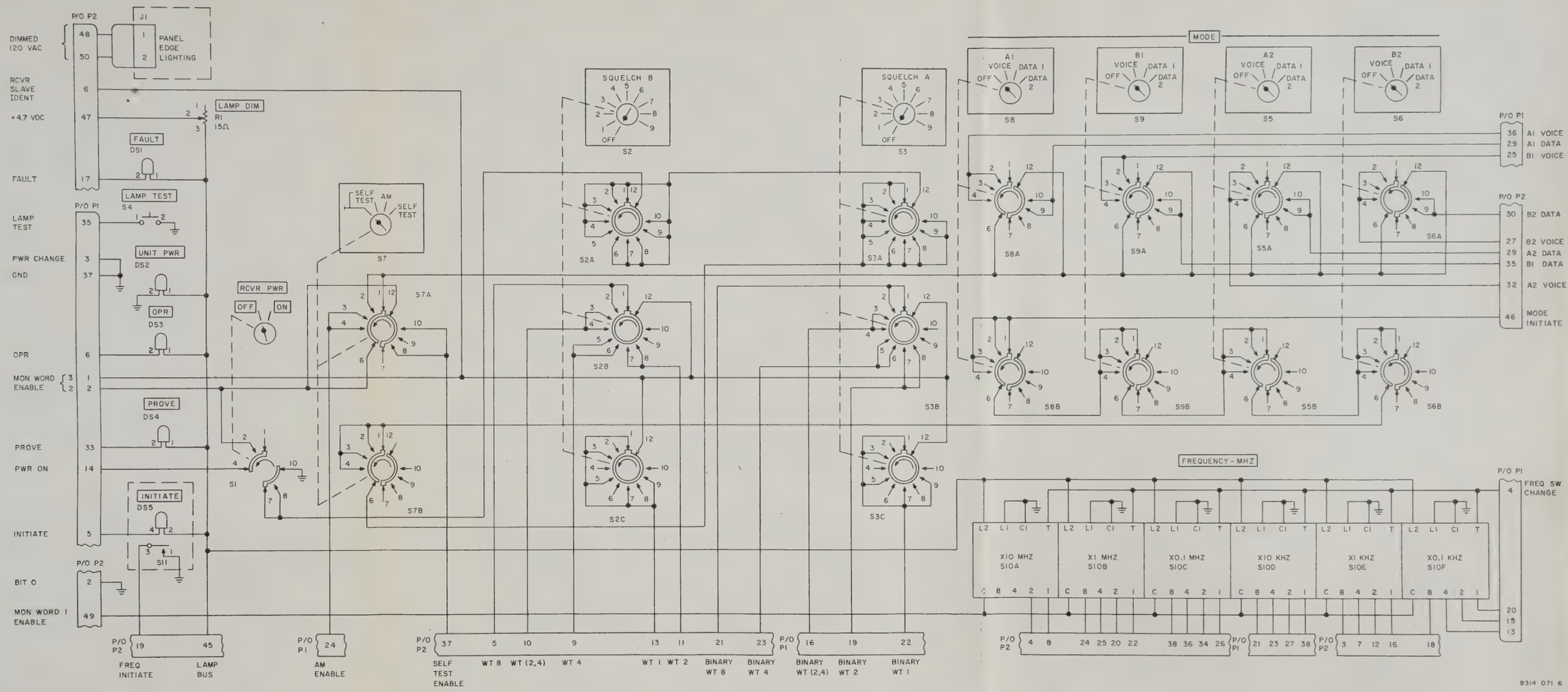
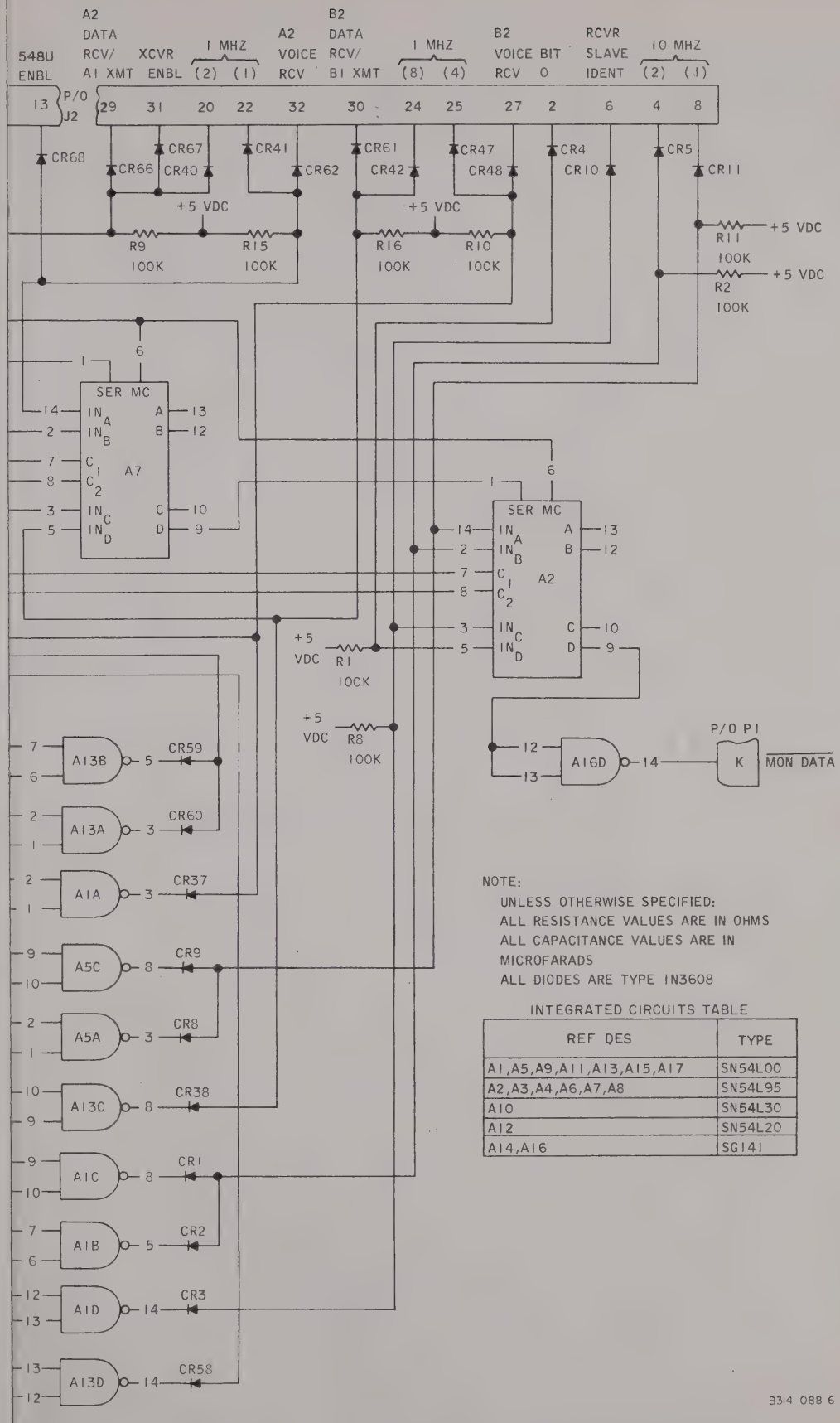


Figure 7-2. Receive Control Head Front Panel, Schematic Diagram



NOTE:
UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE VALUES ARE IN OHMS
ALL CAPACITANCE VALUES ARE IN MICROFARADS
ALL DIODES ARE TYPE IN3608

INTEGRATED CIRCUITS TABLE

REF DES	TYPE
A1,A5,A9,A11,A13,A15,A17	SN54L00
A2,A3,A4,A6,A7,A8	SN54L95
A10	SN54L30
A12	SN54L20
A14,A16	SG141

B3I4 088 6

Figure 7-3. Matrix Card, Detailed Logic Diagram

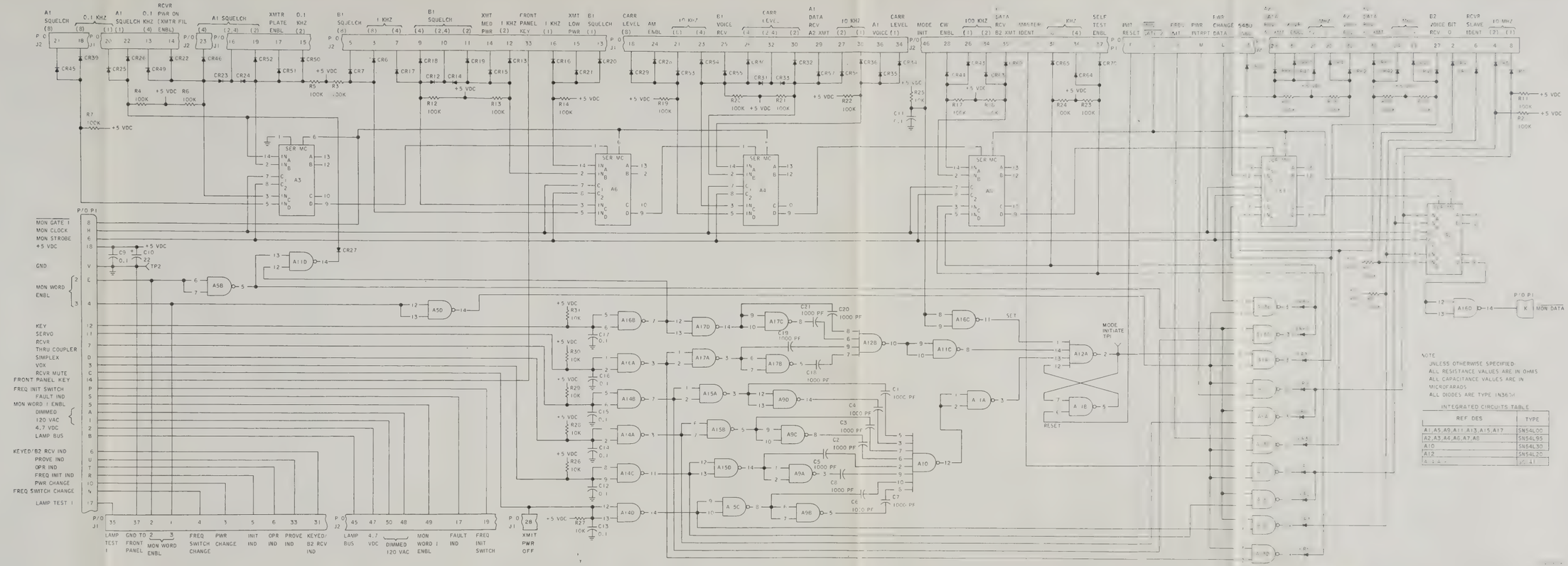


Figure 7-3. Matrix Card, Detailed Logic Diagram

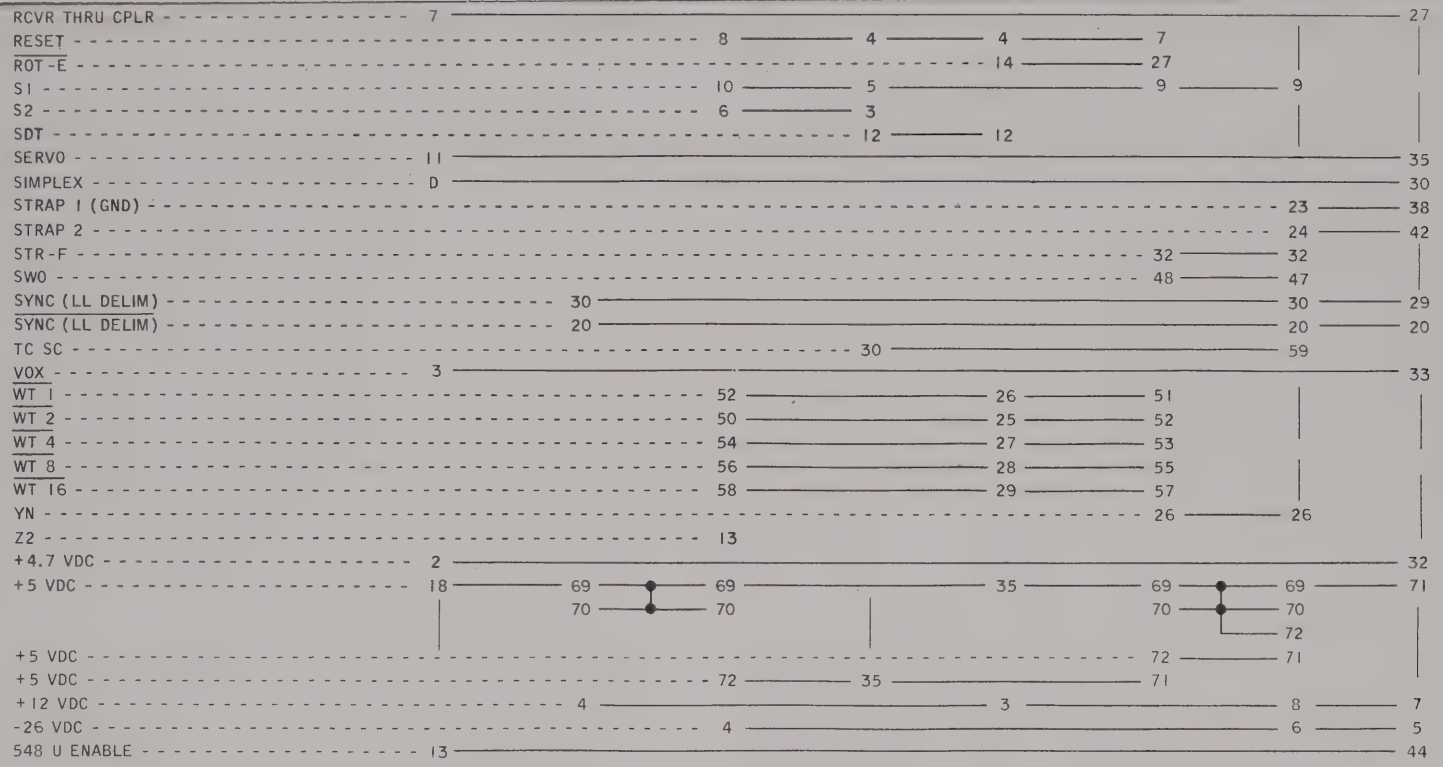


TABLE I. PINS NOT USED

J2	15
A1	21, 22, 55, 57, 71
A2	3, 5, 9, 11, 12, 16, 17, 18, 19, 20, 21, 23, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 41, 43, 45, 49, 51, 55, 57, 59, 60, 61, 63, 66
A3	23, 34
A5	4, 5, 10, 30, 34, 36, 37, 38, 39, 40, 43, 45, 49, 50, 54, 56, 58, 60, 61, 62, 63, 66
A6	41, 49, 53, 54, 60, 62
J1	48, 60, 69

B3I4 080 6

USE OF THE BACKPLANE INTERCONNECT DIAGRAM

THE PURPOSE OF THIS DIAGRAM IS TO SHOW THE ELECTRICAL INTERFACE BETWEEN THE SUBASSEMBLIES THAT PLUG INTO THE BACKPLANE. THE REFERENCE DESIGNATORS OF ALL CONNECTORS LOCATED ON THE BACKPLANE, AND THEIR MATING CONNECTORS ARE LISTED ACROSS THE TOP OF THE DIAGRAM. ALL FUNCTIONS ARE LISTED VERTICALLY DOWN THE LEFT SIDE OF THE DIAGRAM AND ARE IN ALPHABETICAL SEQUENCE. A FUNCTION MAY BE PLACED OUT OF SEQUENCE IF IT IS PHYSICALLY MORE PRATICAL DUE TO STRAPPING ETC.

TO USE THIS DIAGRAM, GO TO THE DESIRED FUNCTION AND TRACK HORIZONTALLY TO DETERMINE WHICH BACKPLANE CONNECTORS THIS FUNCTION IS TIED TO.

Figure 7-4. Backplane Card, Schematic Diagram

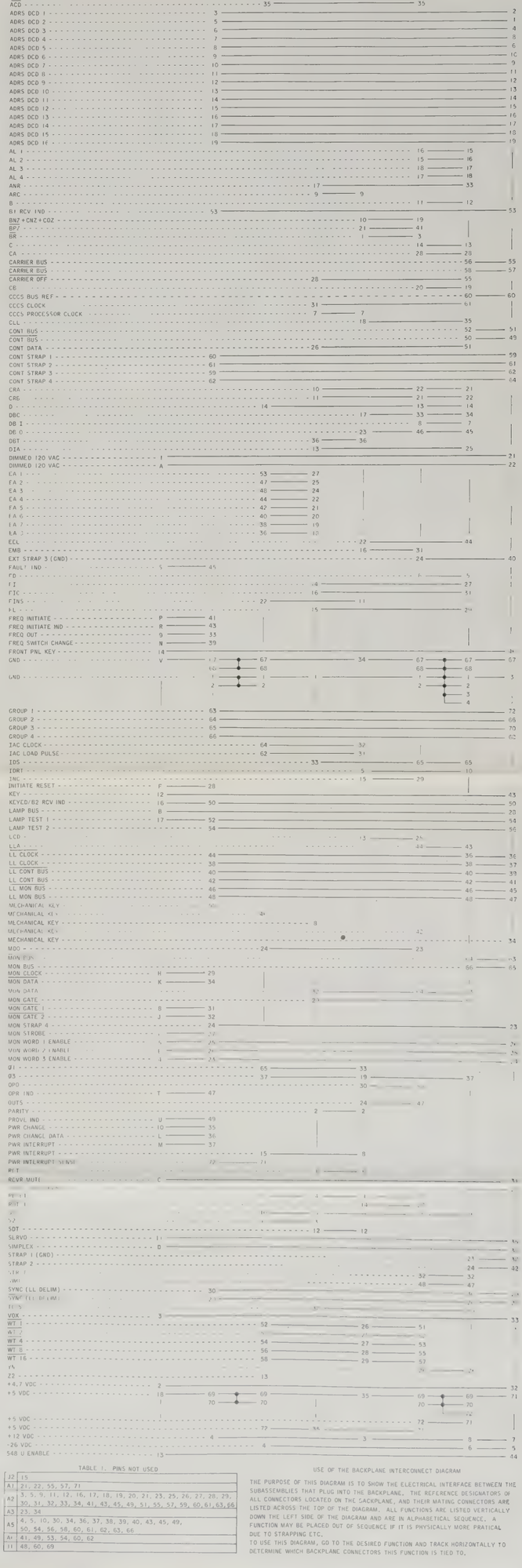


Figure 7-4. Backplane Card, Schematic Diagram

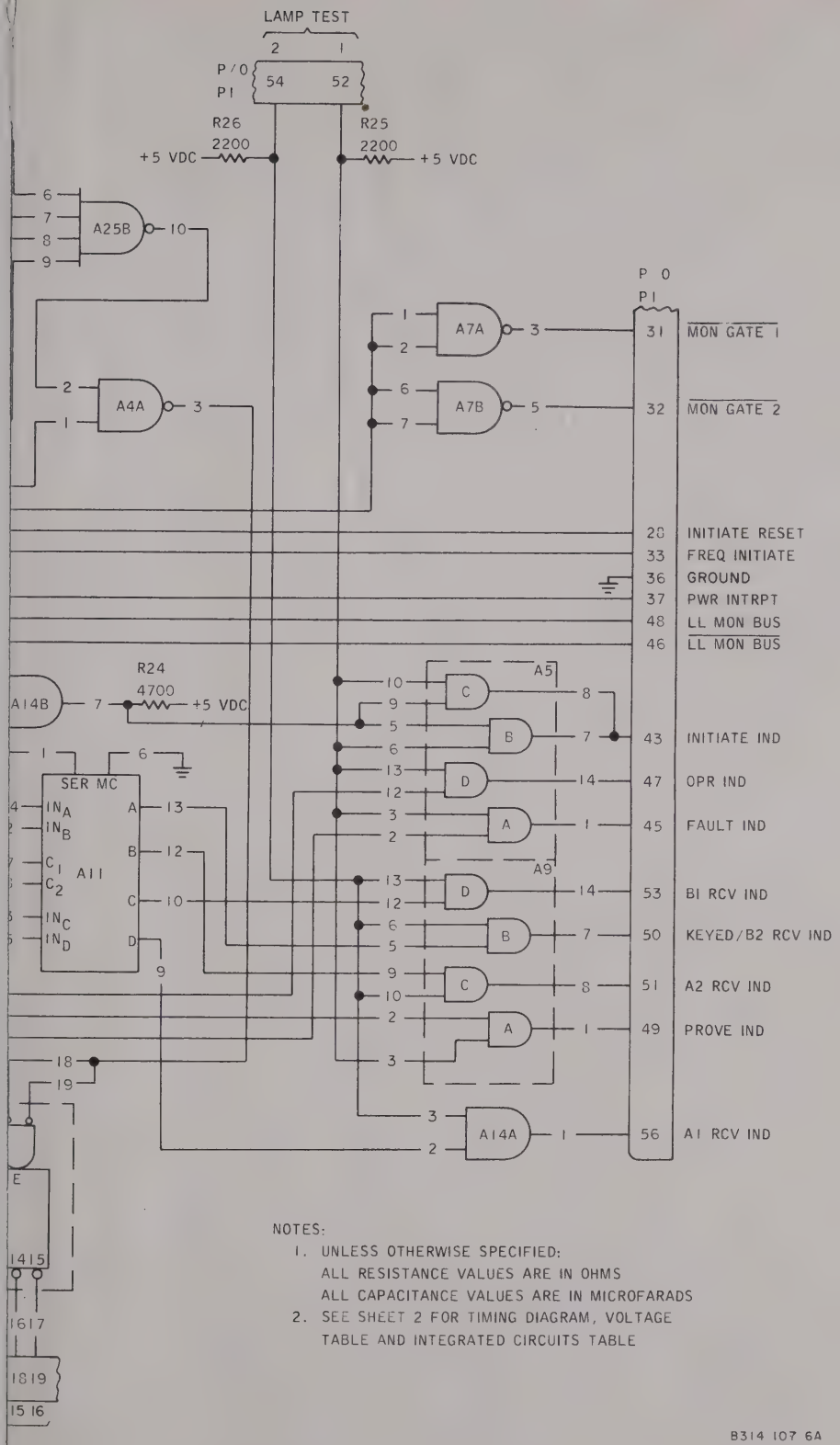
TABLE 1. PINS NOT USED

J2	15
A1	21, 22, 55, 57, 71
A2	3, 5, 9, 11, 12, 16, 17, 18, 19, 20, 21, 23, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 41, 43, 45, 49, 51, 55, 57, 59, 60, 61, 63, 66
A3	23, 34
A5	5, 7, 10, 30, 34, 36, 37, 38, 39, 40, 43, 45, 49, 50, 54, 56, 58, 60, 61, 62, 63, 66
A6	41, 49, 53, 54, 60, 62
J1	48, 60, 69

USE OF THE BACKPLANE INTERCONNECT DIAGRAM

THE PURPOSE OF THIS DIAGRAM IS TO SHOW THE ELECTRICAL INTERFACE BETWEEN THE SUBASSEMBLIES THAT PLUG INTO THE BACKPLANE. THE REFERENCE DESIGNATORS OF ALL CONNECTORS LOCATED ON THE BACKPLANE, AND THEIR MATING CONNECTORS ARE LISTED ACROSS THE TOP OF THE DIAGRAM. ALL FUNCTIONS ARE LISTED VERTICALLY DOWN THE LEFT SIDE OF THE DIAGRAM AND ARE IN ALPHABETICAL SEQUENCE. A FUNCTION MAY BE PLACED OUT OF SEQUENCE IF IT IS PHYSICALLY MORE PRATICAL DUE TO STRAPPING ETC.

TO USE THIS DIAGRAM, GO TO THE DESIRED FUNCTION AND TRACK HORIZONTALLY TO DETERMINE WHICH BACKPLANE CONNECTORS THIS FUNCTION IS TIED TO.



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE IN OHMS
   ALL CAPACITANCE VALUES ARE IN MICROFARADS
2. SEE SHEET 2 FOR TIMING DIAGRAM, VOLTAGE TABLE AND INTEGRATED CIRCUITS TABLE

B314 107 6A

Figure 7-5. Logic Level Slave Card, Detailed Logic Diagram (Sheet 1 of 2)

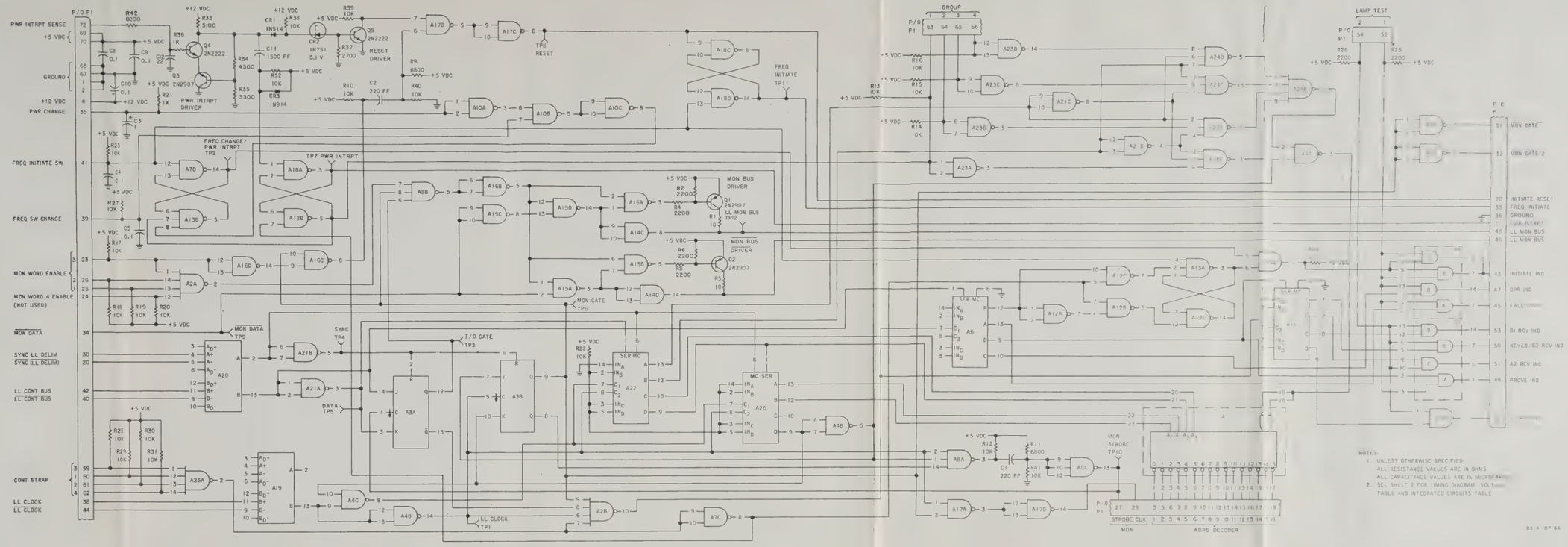
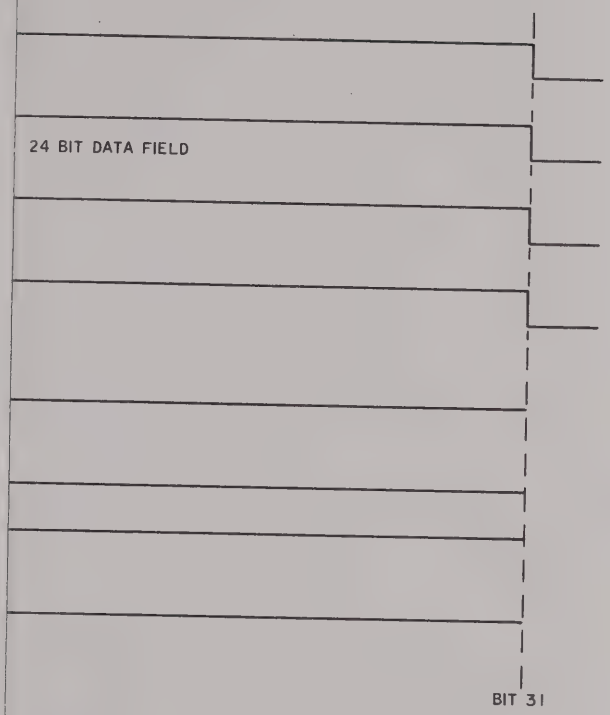


Figure 7-5. Logic Level Slave Card, Detailed Logic Diagram (Sheet 1 of 2)



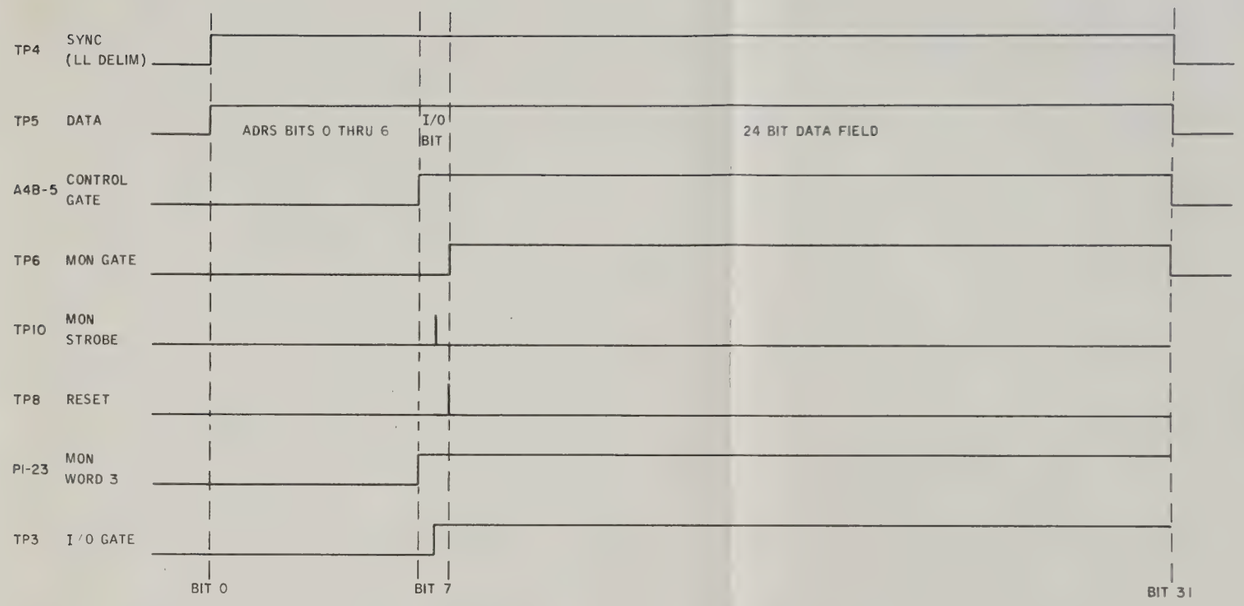
RANSVERSE FROM
T A LOGIC I LEVEL

INTEGRATED CIRCUITS TABLE

REF DES	TYPE
A1	MSI9311
A2,A25	SN54L20
A3	SN54L73
A4,A7,A10,A12,A15,A16,A17,A18,A21,A23	SN54L00
A5,A9,A14	UD4225
A6,A11,A22,A26	SN54L95
A8,A13,A24	SN54L10
A19,A20	FC9620

B314 107 6B

Figure 7-5. Logic Level Slave Card, Detailed Logic Diagram (Sheet 2 of 2)



NOTE:
THE ABOVE SIGNALS ARE TTL GATE OUTPUTS THAT TRANSVERSE FROM OV + 0.5 -OV AT A LOGIC 0 LEVEL TO +3.5 ±0.5V AT A LOGIC 1 LEVEL

TRANSISTOR VOLTAGE TABLE

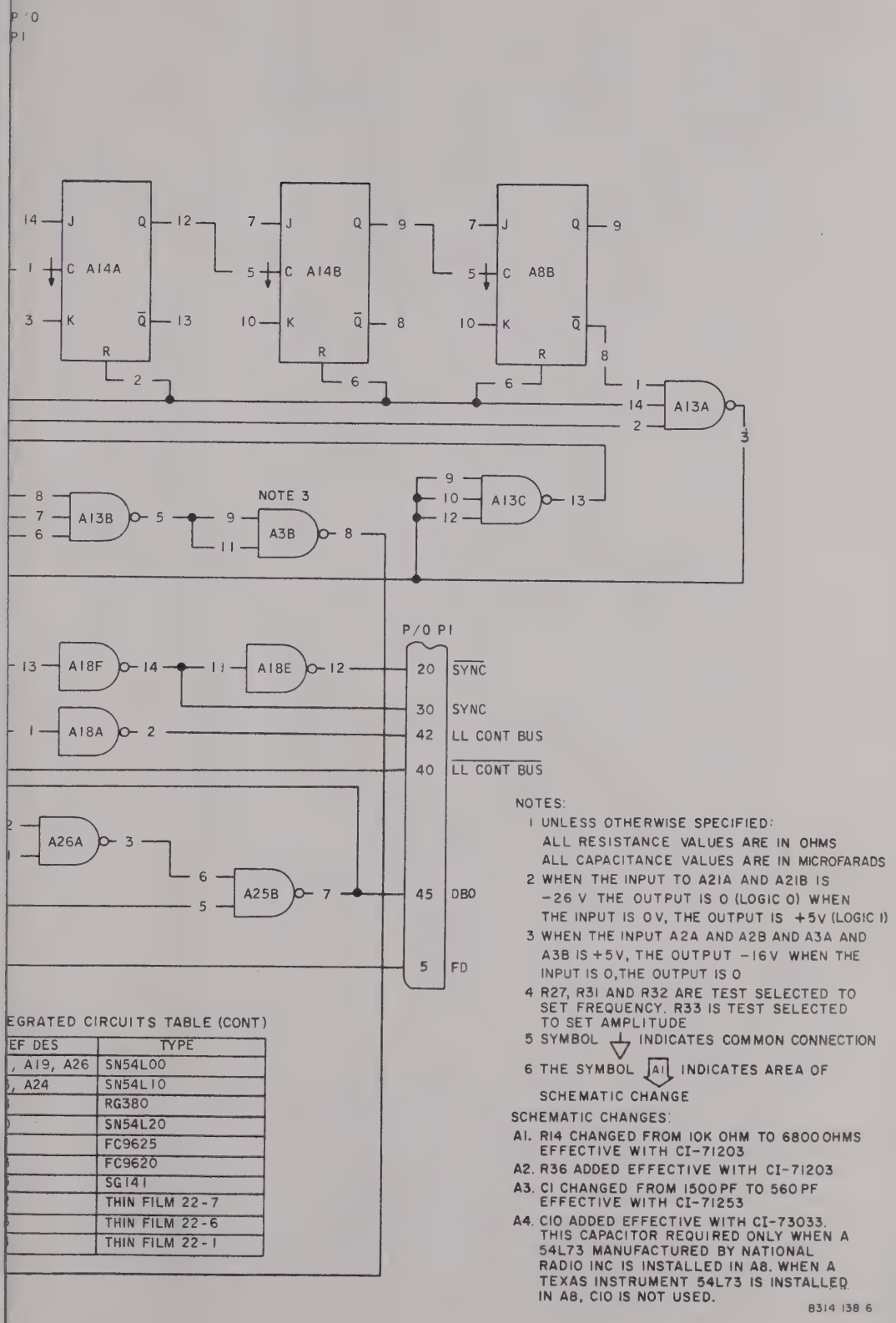
REF DES		VOLTAGE		
		EMITTER	BASE	COLLECTOR
Q1 (PIN 48) Q2 (PIN 46)	(LOGIC "1")	+5.0±0.5	$+4.4^{+0.1}_{-0.2}$	$+4.9^{+0.1}_{-0.3}$
Q1 (PIN 48) Q2 (PIN 46)	(LOGIC "0")	+5.0±0.5	+5.0±0.5	$+0.5^{+0.0}_{-0.45}$
Q3		+1.2±0.3	+0.6±0.2	0 (GND)
Q4		+1.2±0.2	+1.8±0.2	+1.5±0.2
Q5		0 (GND)	$-0.1^{+0.2}_{-0.0}$	$+5.0^{+0.5}_{-1.0}$

INTEGRATED CIRCUITS TABLE

REF DES	TYPE
A1	MSI9311
A2,A25	SN54L20
A3	SN54L73
A4,A7,A10,A12,A15,A16,A17,A18,A21,A23	SN54L00
A5,A9,A14	UD4225
A6,A11,A22,A26	SN54L95
A8,A13,A24	SN54L10
A19,A20	FC9620

8314 107 68

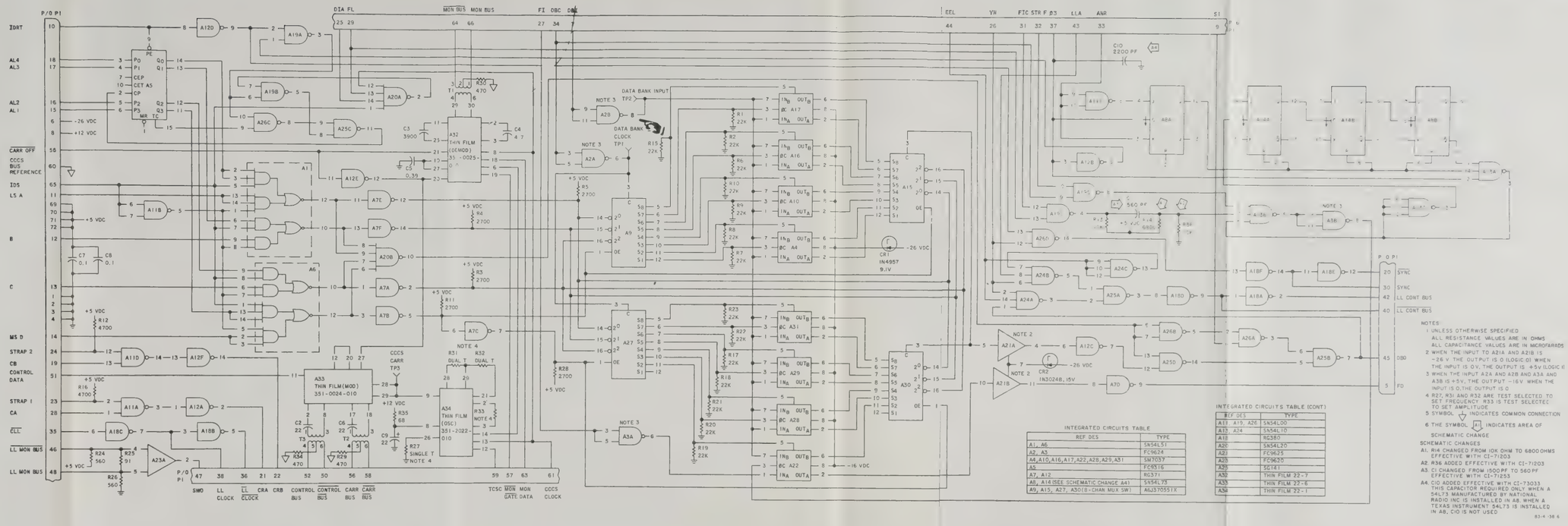
Figure 7-5. Logic Level Slave Card, Detailed Logic Diagram (Sheet 2 of 2)



EGRATED CIRCUITS TABLE (CONT)

EF DES	TYPE
, A19, A26	SN54L00
, A24	SN54L10
	RG380
	SN54L20
	FC9625
	FC9620
	SG141
	THIN FILM 22-7
	THIN FILM 22-6
	THIN FILM 22-1

Figure 7-6. Accessible Memory Card, Detailed Logic Diagram



NOTES:

1. UNLESS OTHERWISE SPECIFIED ALL RESISTANCE VALUES ARE IN OHMS ALL CAPACITANCE VALUES ARE IN MICROFARADS
2. WHEN THE INPUT TO A21A AND A21B IS −26 V THE OUTPUT IS 0 (LOGIC 0) WHEN THE INPUT IS 0 V, THE OUTPUT IS +5V (LOGIC 1)
3. WHEN THE INPUT A2A AND A2B AND A3A AND A3B IS +5V, THE OUTPUT −16V WHEN THE INPUT IS 0, THE OUTPUT IS 0
4. R27, R31 AND R32 ARE TEST SELECTED TO SET FREQUENCY. R33 IS TEST SELECTED TO SET AMPLITUDE
5. SYMBOL ⏚ INDICATES COMMON CONNECTION
6. THE SYMBOL A1 INDICATES AREA OF SCHEMATIC CHANGE

SCHEMATIC CHANGES

A1. R14 CHANGED FROM 10K OHM TO 6800 OHMS EFFECTIVE WITH CI-71203
A2. R36 ADDED EFFECTIVE WITH CI-71203
A3. C1 CHANGED FROM 1500 PF TO 560 PF EFFECTIVE WITH CI-71253
A4. C10 ADDED EFFECTIVE WITH CI-73033 THIS CAPACITOR REQUIRED ONLY WHEN A 54L73 MANUFACTURED BY NATIONAL RADIO INC IS INSTALLED IN A8. WHEN A TEXAS INSTRUMENT 54L73 IS INSTALLED IN A8, C10 IS NOT USED

83-4-38 6

INTEGRATED CIRCUITS TABLE

REF DES	TYPE
A1, A6	SN54L51
A2, A3	FC9624
A4, A10, A16, A17, A22, A28, A29, A31	SM7037
A5	FC9316
A7, A12	RG371
A8, A14 (SEE SCHEMATIC CHANGE A4)	SN54L73
A9, A15, A27, A30 (8-CHAN MUX SW)	A6J370551X

INTEGRATED CIRCUITS TABLE (CONT)

REF DES	TYPE
A11, A19, A26	SN54L00
A13, A24	SN54L10
A18	RG380
A20	SN54L20
A21	FC9625
A23	FC9620
A25	SG141
A32	THIN FILM 22-7
A33	THIN FILM 22-6
A34	THIN FILM 22-1

Figure 7-6. Accessible Memory Card, Detailed Logic Diagram

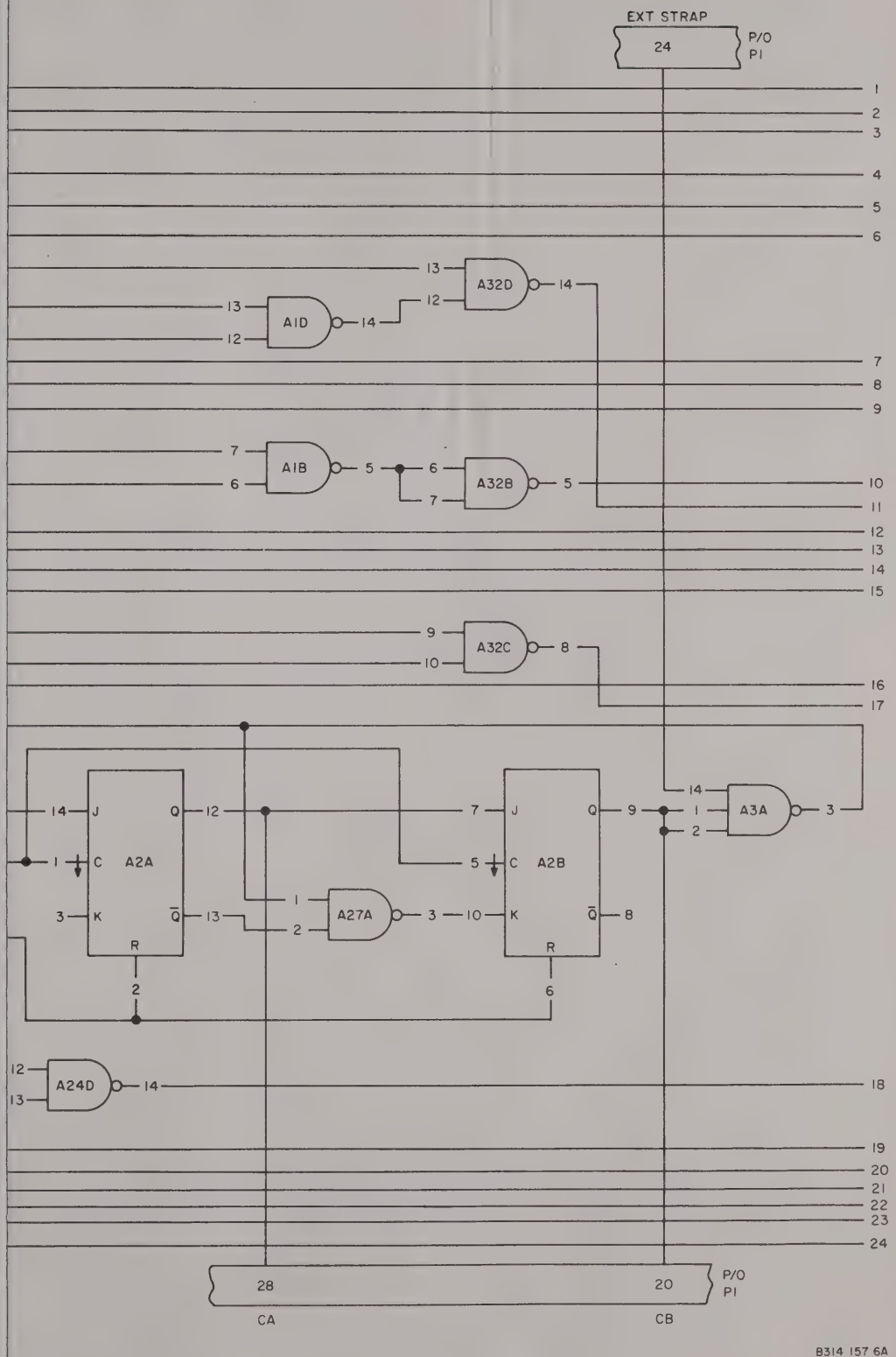


Figure 7-7. Instruction Decode Card, Detailed Logic Diagram (Sheet 1 of 2)

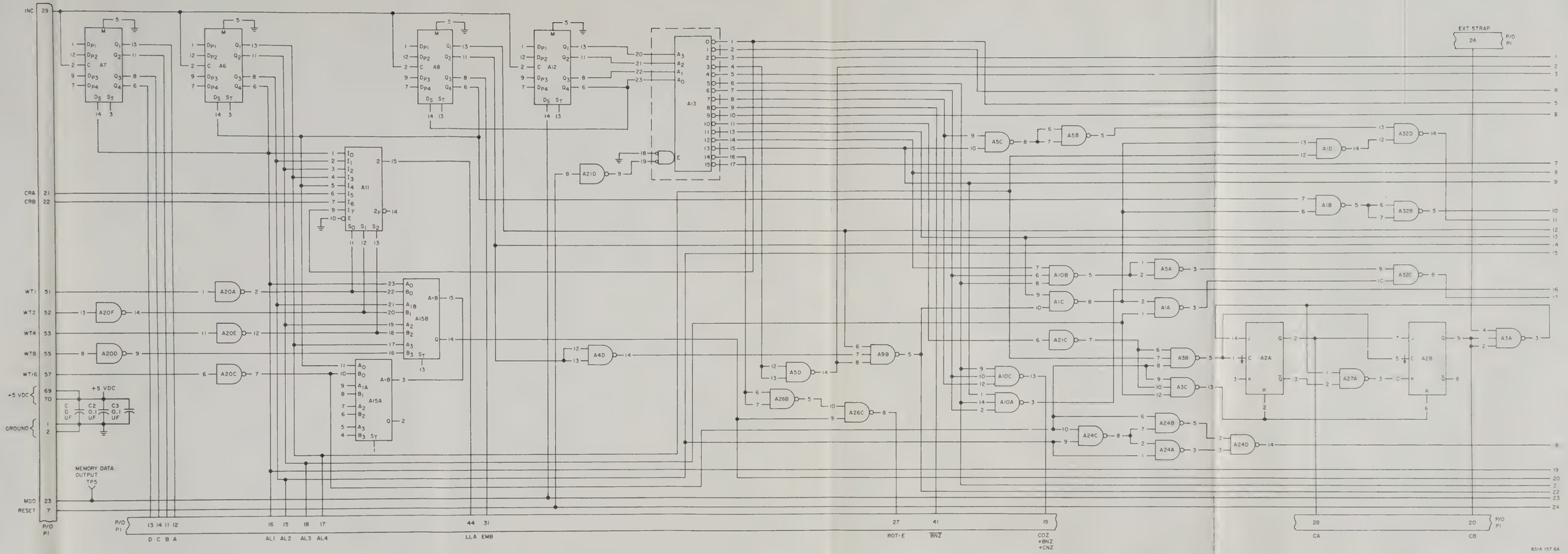
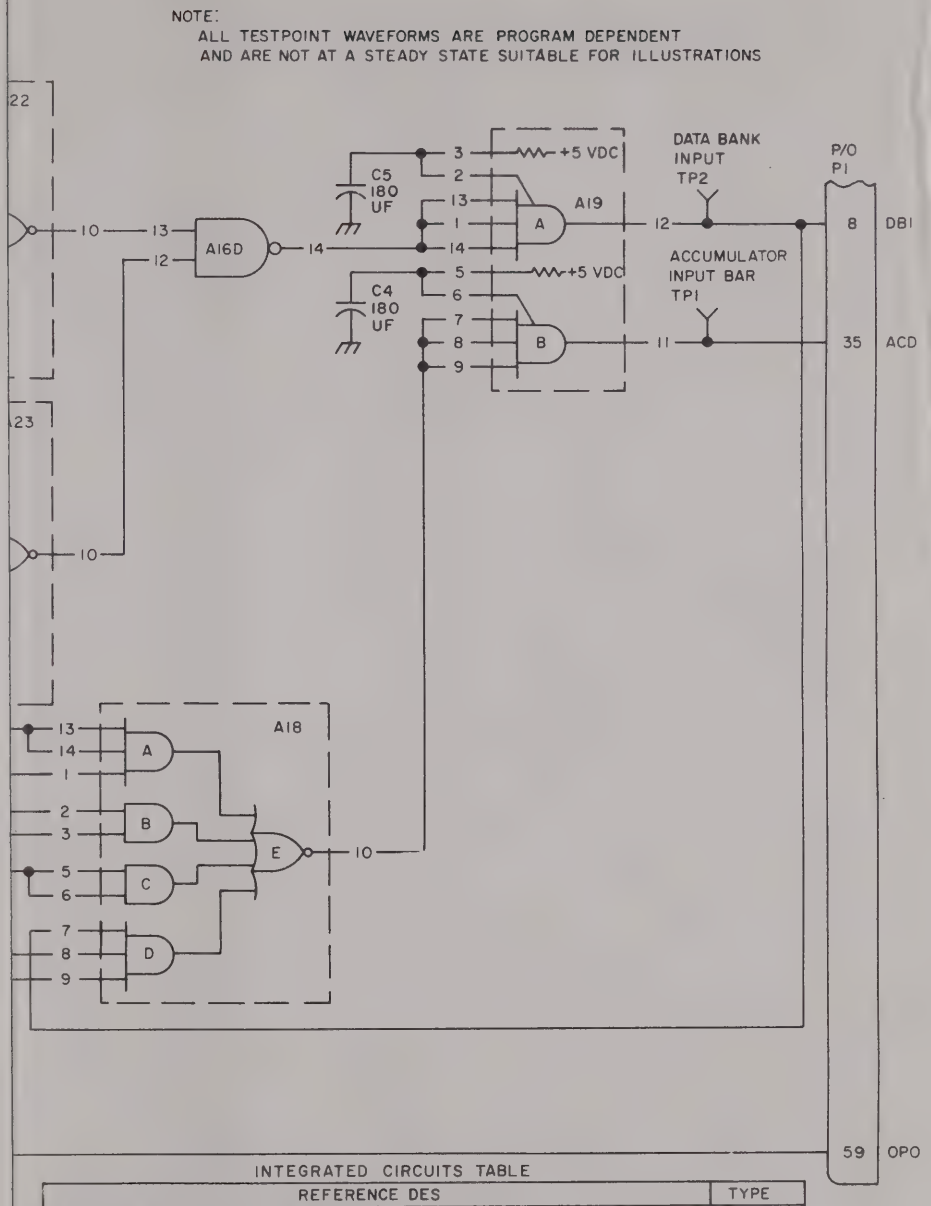


Figure 7-7. Instruction Decode Card, Detailed Logic Diagram (Sheet 1 of 2)

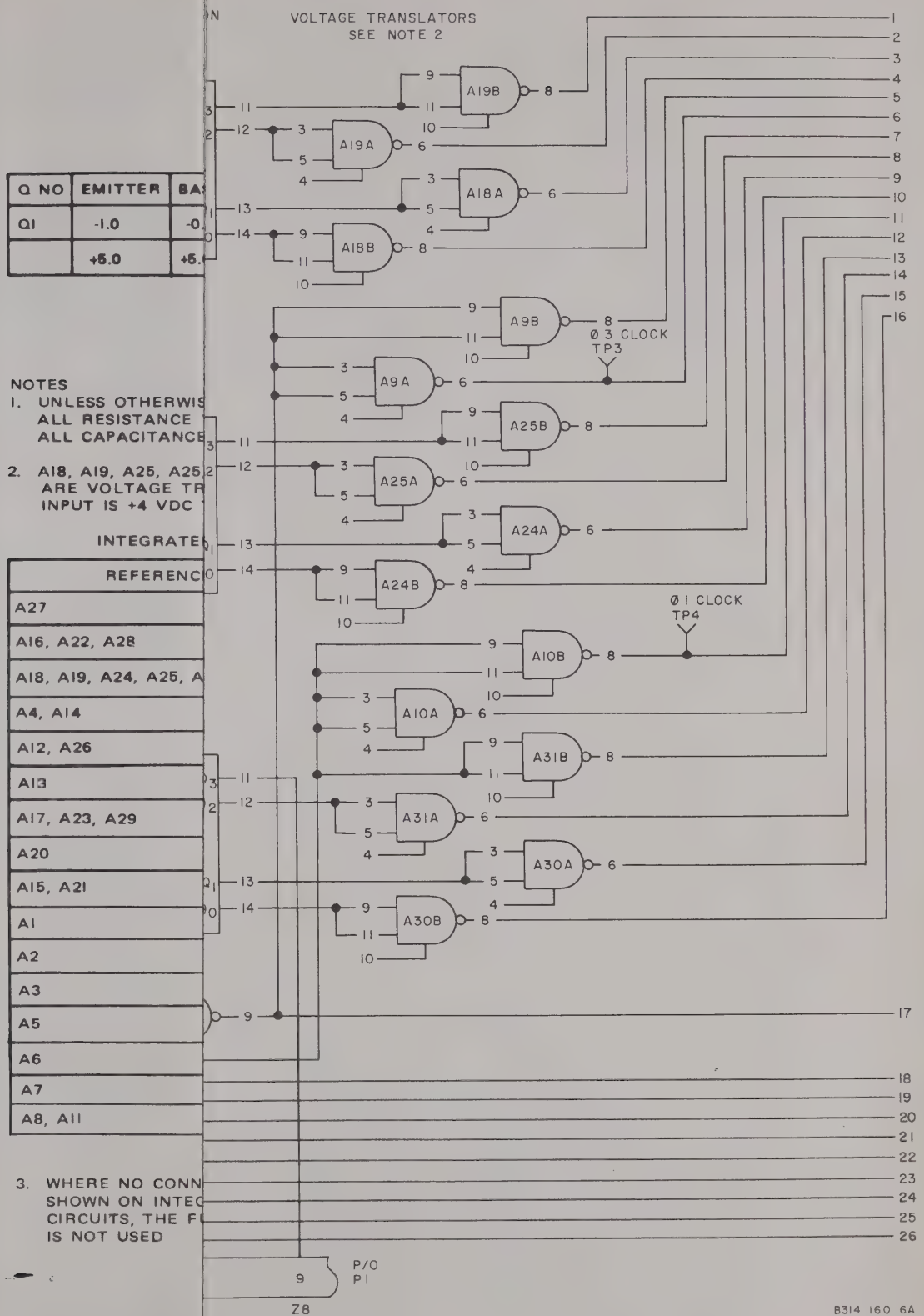


INTEGRATED CIRCUITS TABLE

REFERENCE DES	TYPE
A1, A4, A5, A14, A17, A24, A25, A26, A27, A29, A32	SN54L00
A3, A9, A10	SN54L10
A18, A22, A23, A28, A30	SN54L54
A33	SN54L72
A2	SN54L73
A16	SG141
A31	SM20
A6, A7, A8, A12	SS314
A13	FC9311
A15	FC4510
A11	FC9312
A19	SG81
A20, A21	RG371

B314 157 68

Figure 7-7. Instruction Decode Card, Detailed Logic Diagram (Sheet 2 of 2)



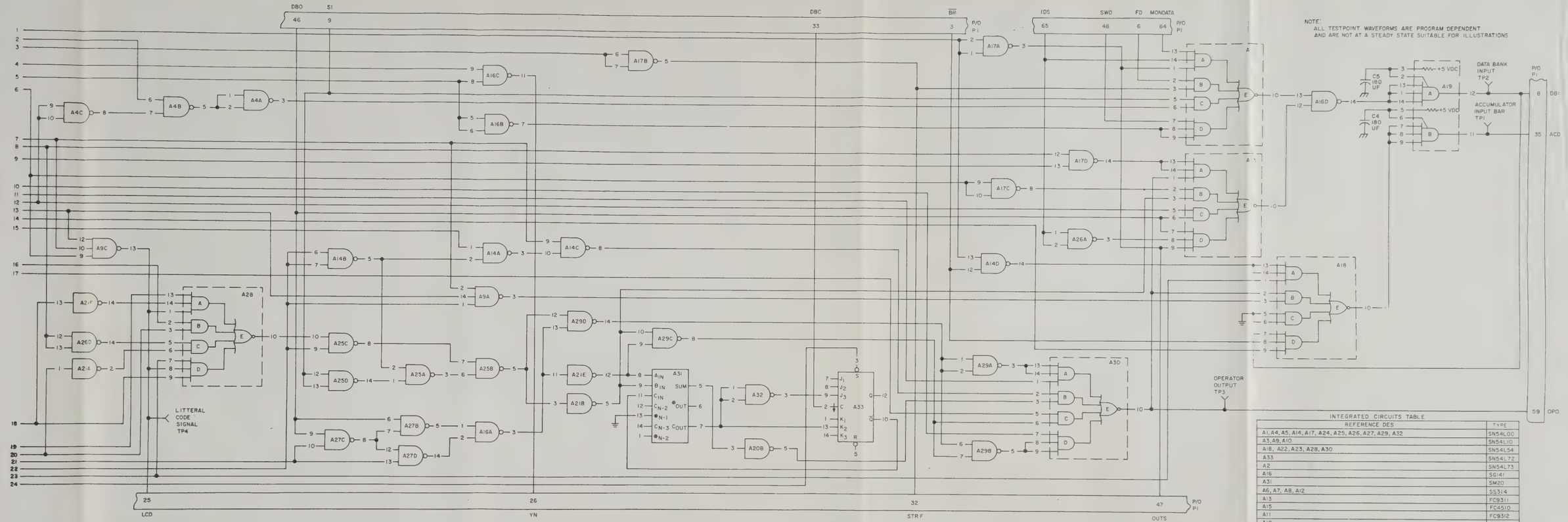
Q NO	EMITTER	BA
Q1	-1.0	-0.
	+5.0	+5.

NOTES
1. UNLESS OTHERWIS
ALL RESISTANCE
ALL CAPACITANCE
2. A18, A19, A25, A25
ARE VOLTAGE TR
INPUT IS +4 VDC
INTEGRATE

REFERENC
A27
A16, A22, A28
A18, A19, A24, A25, A
A4, A14
A12, A26
A13
A17, A23, A29
A20
A15, A21
A1
A2
A3
A5
A6
A7
A8, A11

3. WHERE NO CONN
SHOWN ON INTEG
CIRCUITS, THE F
IS NOT USED

Figure 7-8. Hardwire Memory Card (789-2620-001) Detailed Logic Diagram (Sheet 1 of 2)



INTEGRATED CIRCUITS TABLE

REFERENCE DES	TYPE
A1, A4, A5, A14, A17, A24, A25, A26, A27, A29, A32	SN54L00
A3, A9, A10	SN54L10
A18, A22, A23, A28, A30	SN54L54
A33	SN54L72
A2	SN54L73
A16	SG141
A31	SM20
A6, A7, A8, A12	SS314
A13	FC9311
A15	FC4510
A11	FC9312
A19	SG81
A20, A21	RG371

B3I4 157 68

Figure 7-7. Instruction Decode Card, Detailed Logic Diagram (Sheet 2 of 2)

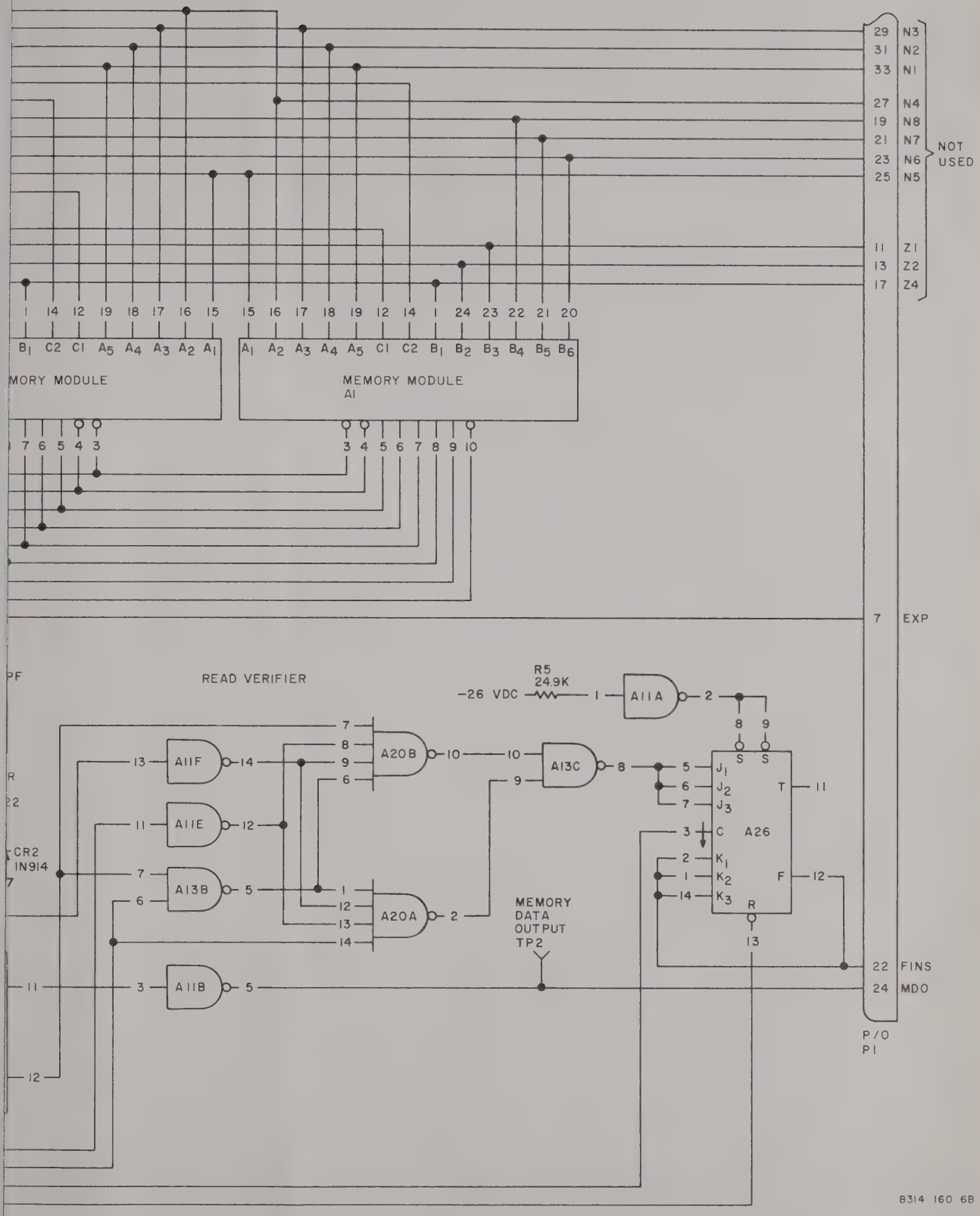


Figure 7-8. Hardwire Memory Card (789-2620-001) Detailed Logic Diagram (Sheet 2 of 2)

Q NO	EMITTER	BASE	COLLECTOR	
Q1	-1.0	-0.3	-0.7	LOGIC 1 OUTPUT
	+5.0	+5.0	+5.0	LOGIC 0 OUTPUT

NOTES
1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTANCE VALUES ARE IN OHMS
   ALL CAPACITANCE VALUES ARE IN MICROFARADS
2. A18, A19, A25, A25, A30, A31, A9 AND A10 ARE VOLTAGE TRANSLATORS. WHEN THE INPUT IS +4 VDC THE OUTPUT IS -26 VDC

INTEGRATED CIRCUITS TABLE

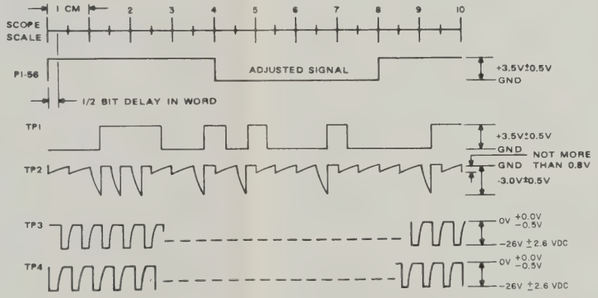
REFERENCE DES	TYPE
A27	SN54L95
A16, A22, A28	SS314
A18, A19, A24, A25, A30, A31, A9, A10	F9624
A4, A14	F3708
A12, A26	SF51
A13	SN54L00
A17, A23, A29	FC9316
A20	SN54L20
A15, A21	SN54L91
A1	MEM2048A
A2	MEM2048C
A3	MEM2048E
A5	MEM2048B
A6	MEM2048D
A7	MEM2048F
A8, A11	RG371

3. WHERE NO CONNECTION IS SHOWN ON INTEGRATED CIRCUITS, THE FUNCTION IS NOT USED

4. TO OBSERVE A STATIONARY SIGNAL AT TP1 AND TP2
   A. TIE P1-64 TO GROUND AT P1-2
   B. SYNC SCOPE ON P1-56 (POS)
   C. DISPLAY SIGNAL AT P1-56 ON TRACE A AND OBSERVE

D. DISPLAY 1 POSITIVE GOING CYCLE ON TRACE A AS SHOWN

E. ADJUST VERNIER TO DISPLAY 1 CYCLE ON 8 CM. THIS PROCEDURE MAKES IT EASIER TO OBSERVE TP1 AND TP2 SIGNALS AS EACH BIT POSITION WILL TAKE 1/2 CM



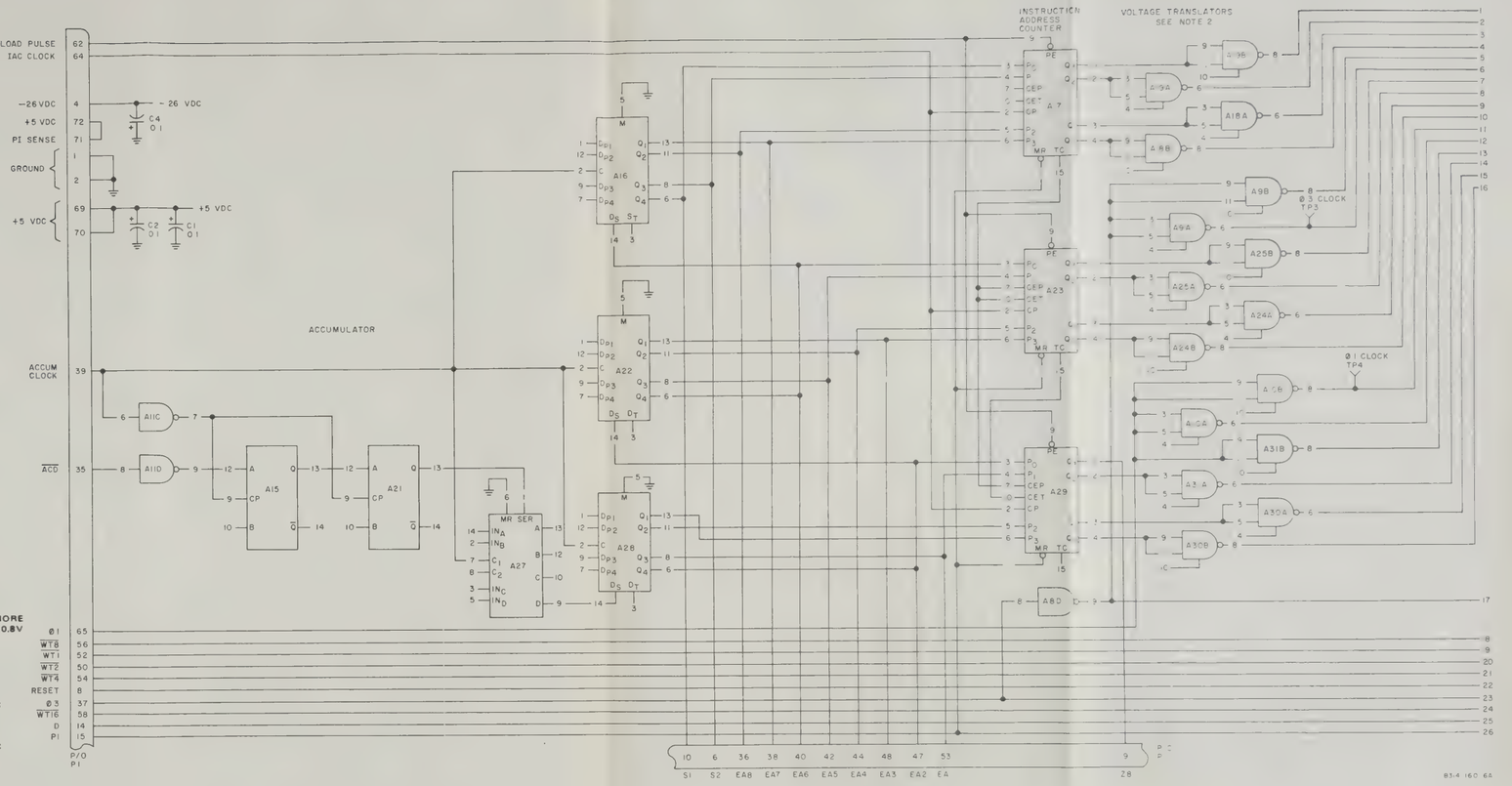


Figure 7-8. Hardwire Memory Card (789-2620-001) Detailed Logic Diagram (Sheet 1 of 2)

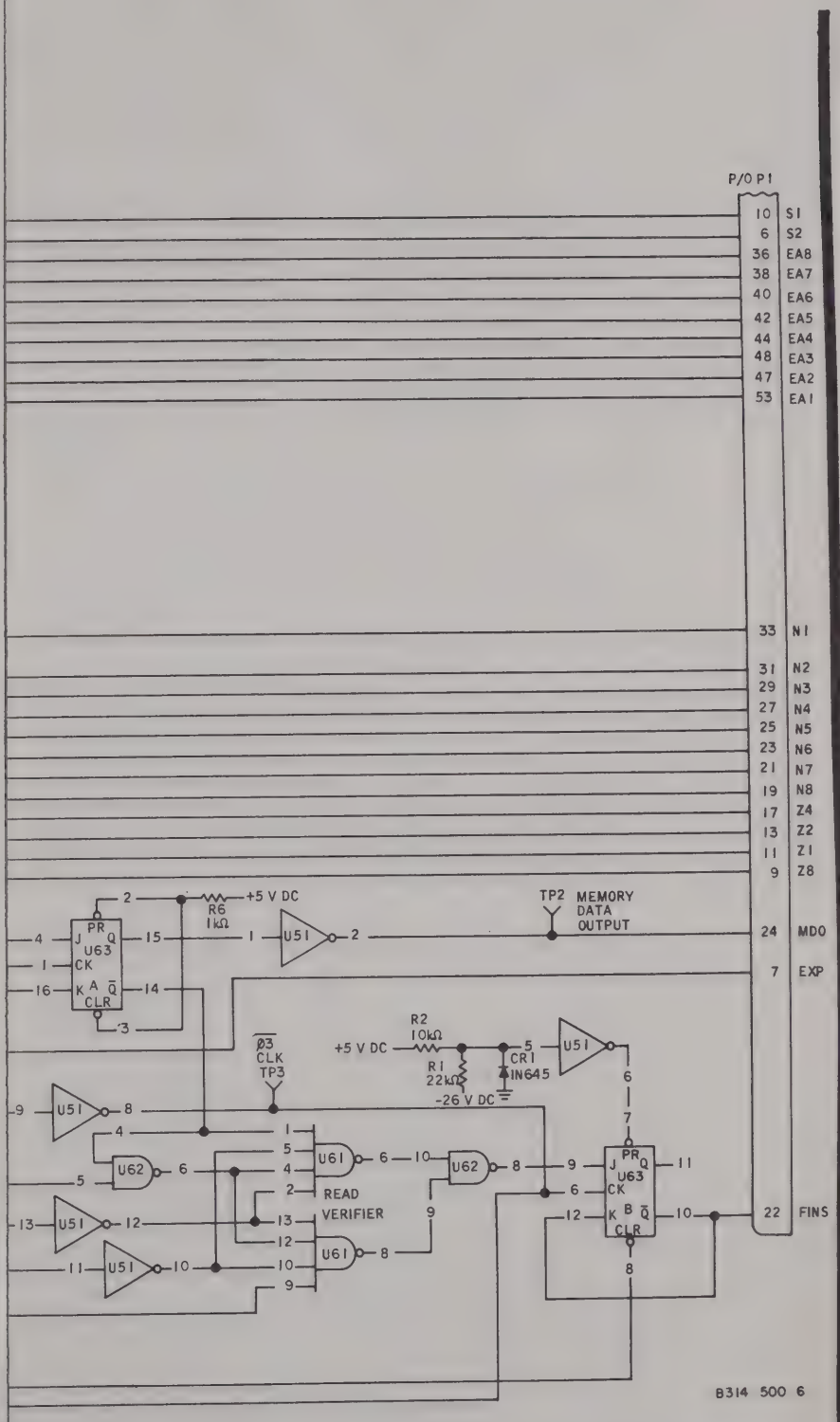


Figure 7-8A. Hardwire Memory Card (633-9332-001), Detailed Logic Diagram

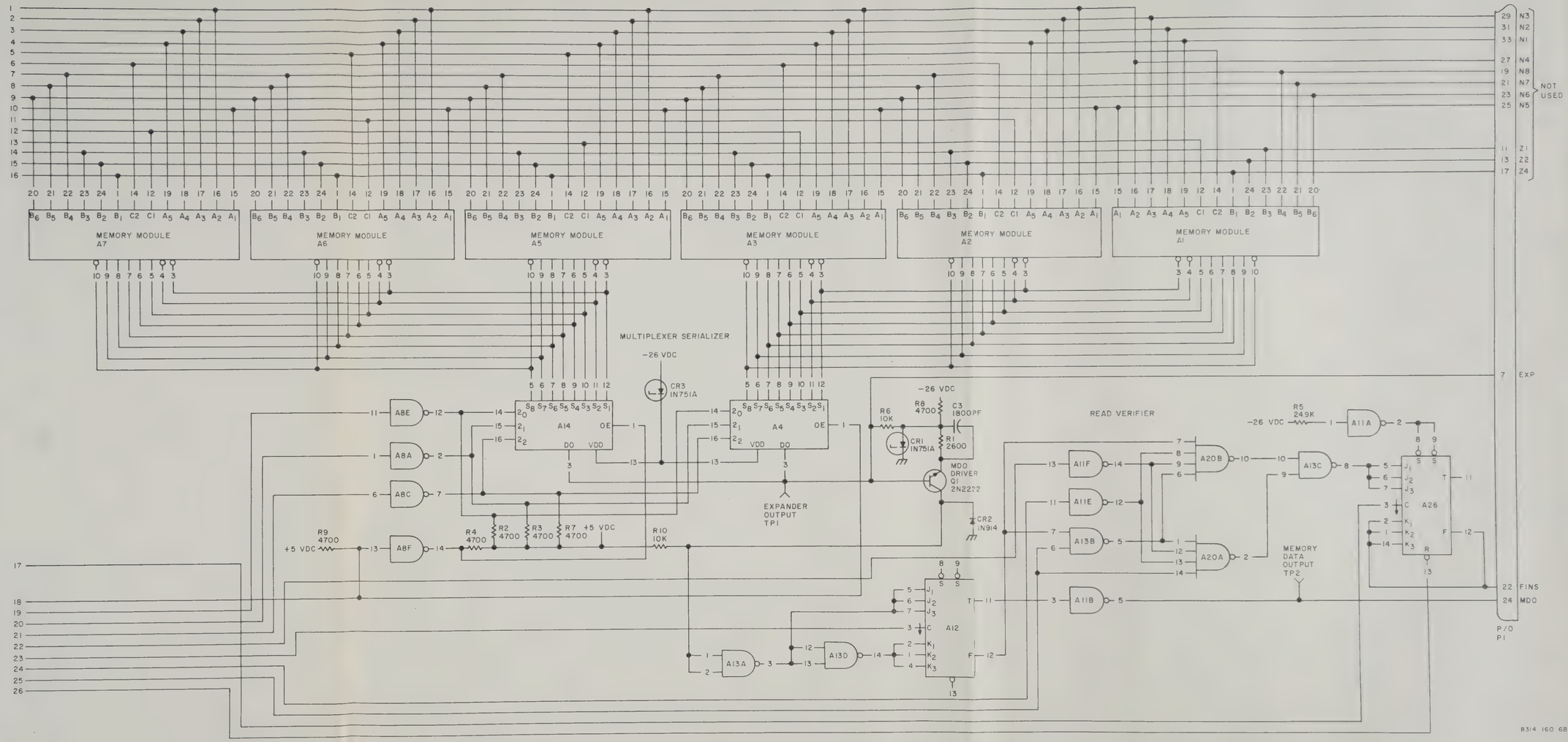


Figure 7-8. Hardwire Memory Card (789-2620-001) Detailed Logic Diagram (Sheet 2 of 2)

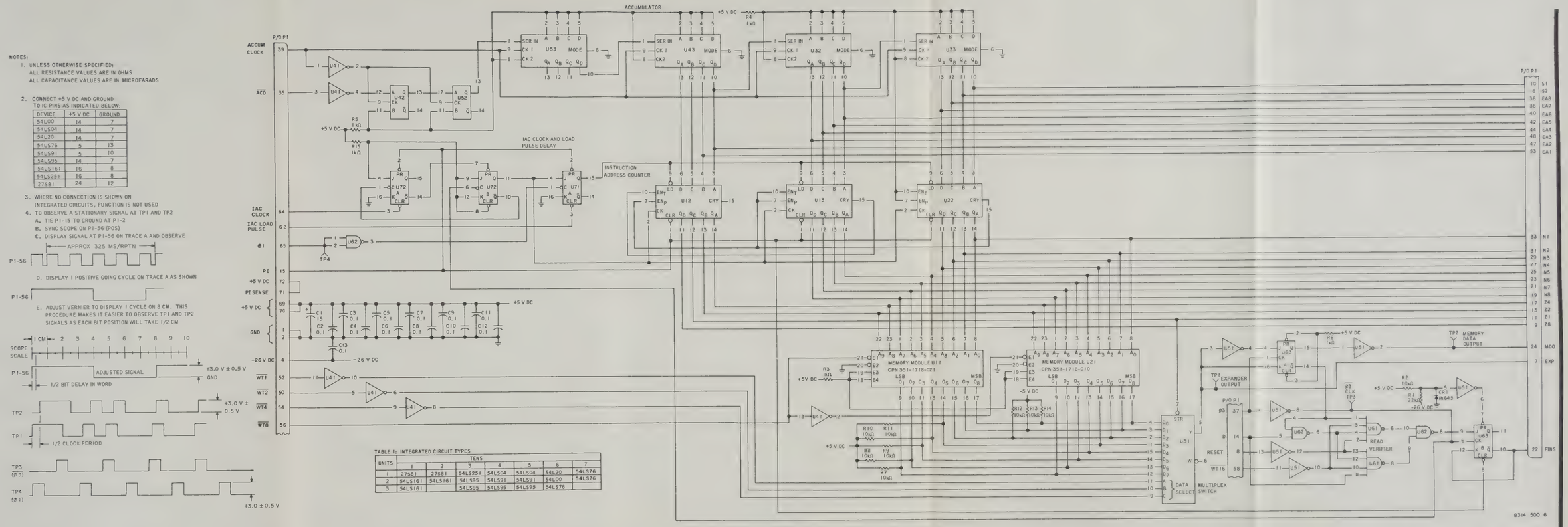


TABLE 1: INTEGRATED CIRCUIT TYPES

UNITS	TENS						
	1	2	3	4	5	6	7
1	27S81	27S81	54LS251	54LS04	54LS04	54L20	54LS76
2	54LS161	54LS161	54LS95	54LS91	54LS91	54L00	54LS76
3	54LS161		54LS95	54LS95	54LS95	54LS76	

Figure 7-8A. Hardwire Memory Card (633-9332-001), Detailed Logic Diagram

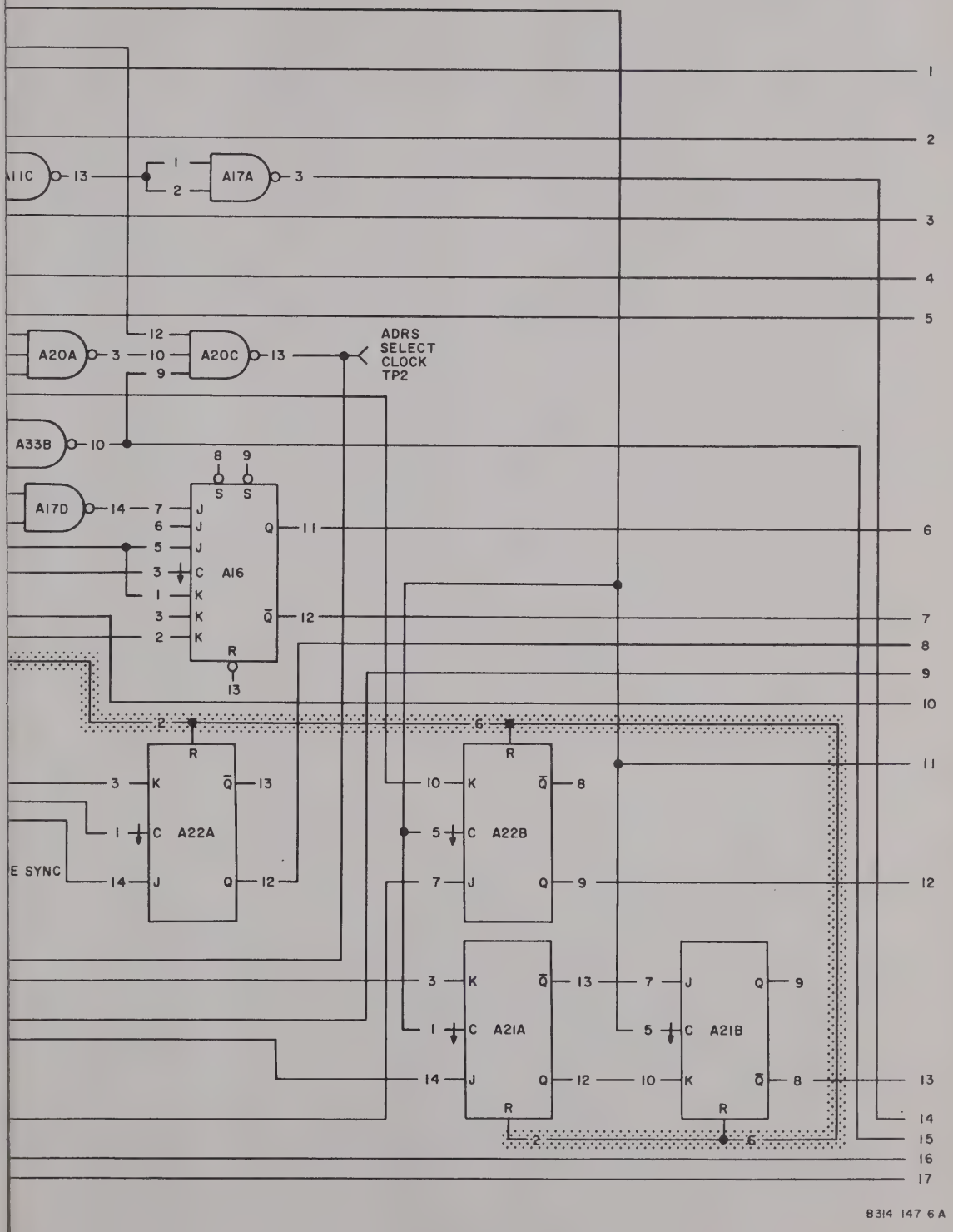


Figure 7-9. CCCS Timing Card, Detailed Logic Diagram (Sheet 1 of 2)

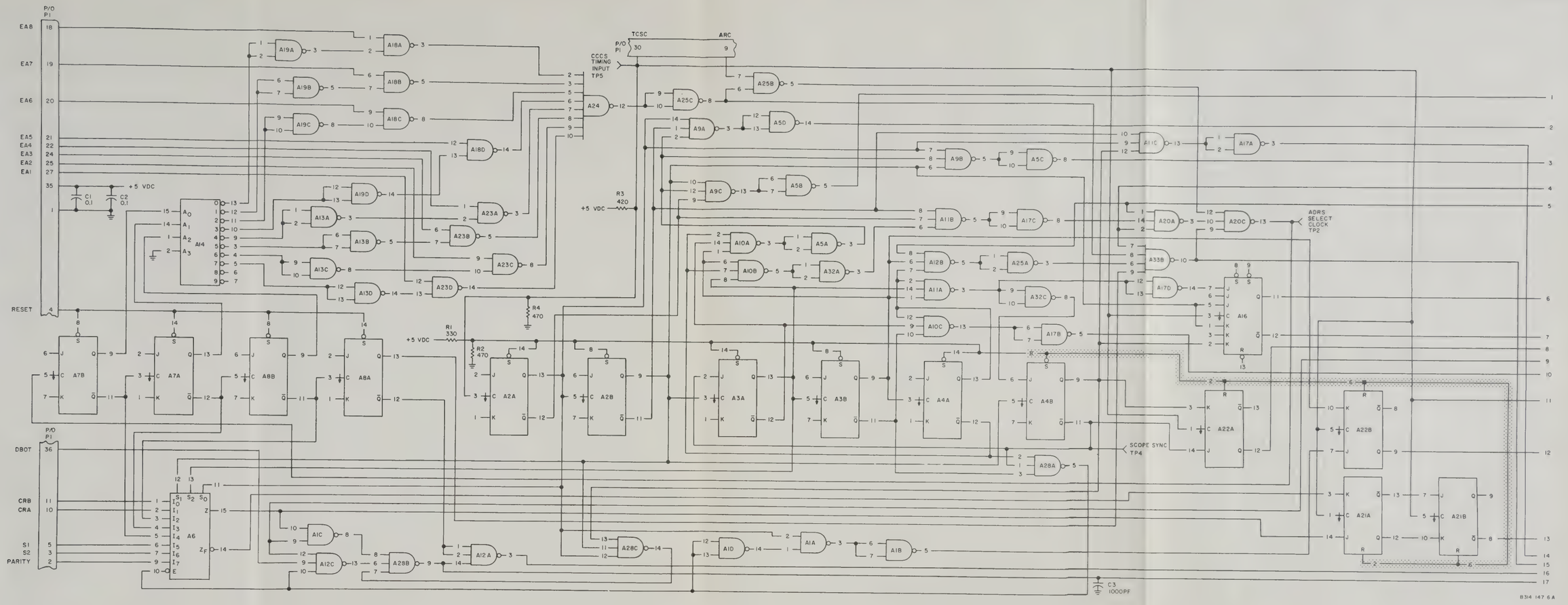
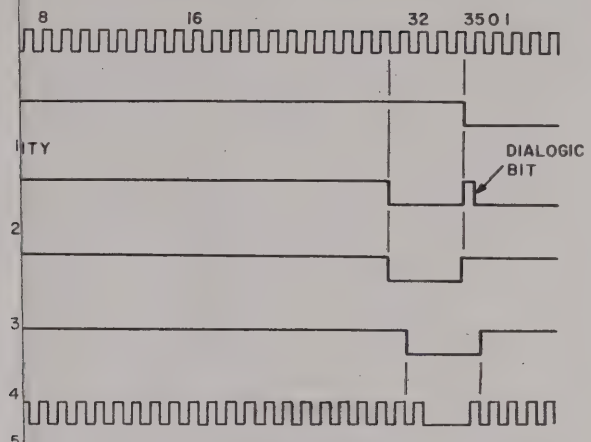


Figure 7-9. CCCS Timing Card, Detailed Logic Diagram (Sheet 1 of 2)



S:
UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE VALUES ARE IN OHMS
ALL CAPACITANCE VALUES ARE IN MICROFARADS
INTEGRATED CIRCUITS IDENTIFICATION
(SEE INTEGRATED CIRCUITS TABLE)

INTEGRATED CIRCUITS TABLE

REFERENCE DES	TYPE
5, A13, A17, A18, A19, A23, A25, , A30, A31, A32	SN54L00
A3, A4, A7, A8	SF101
	MSI9312
10, A11, A12, A20, A26	SN54L10
	MSI9301
A21, A22, A27, A34, A36	SN54L73
	SF51
	SN54L30
	SG191
A35, A37	SN54L20

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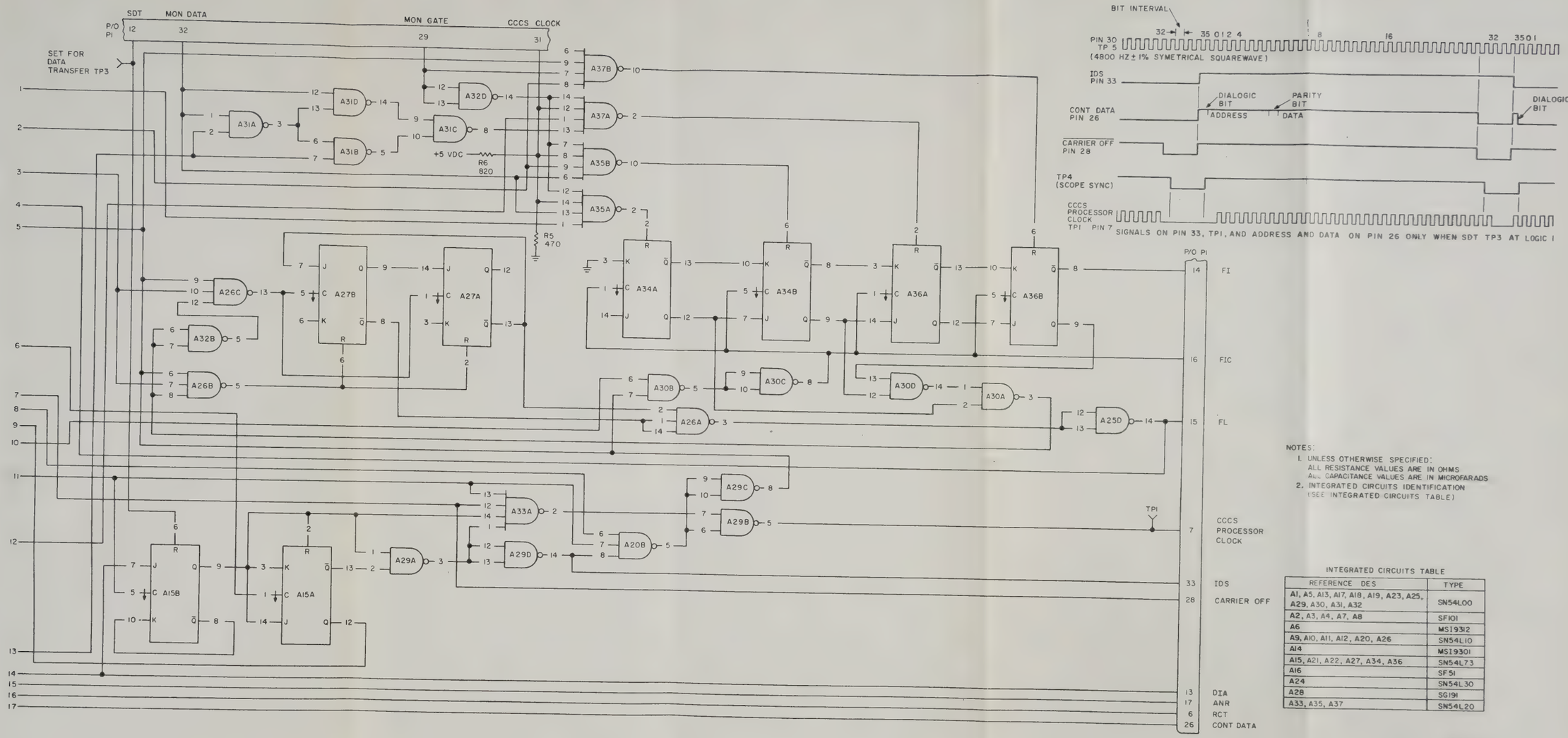
ng Card, Detailed
am (Sheet 2 of 2)



INTEGRATED CIRCUITS TABLE

REFERENCE DES	TYPE
A1, A5, A13, A17, A18, A19, A23, A25, A29, A30, A31, A32	SN54L00
A2, A3, A4, A7, A8	SF101
A6	MS1932
A9, A10, A11, A12, A20, A26	SN54L10
A14	MS1930
A15, A21, A22, A27, A34, A36	SN54L73
A16	SF51
A24	SN54L30
A28	SG191
A33, A35, A37	SN54L20

Figure 7-9. CCCS Timing Card, Detailed Logic Diagram (Sheet 2 of 2)

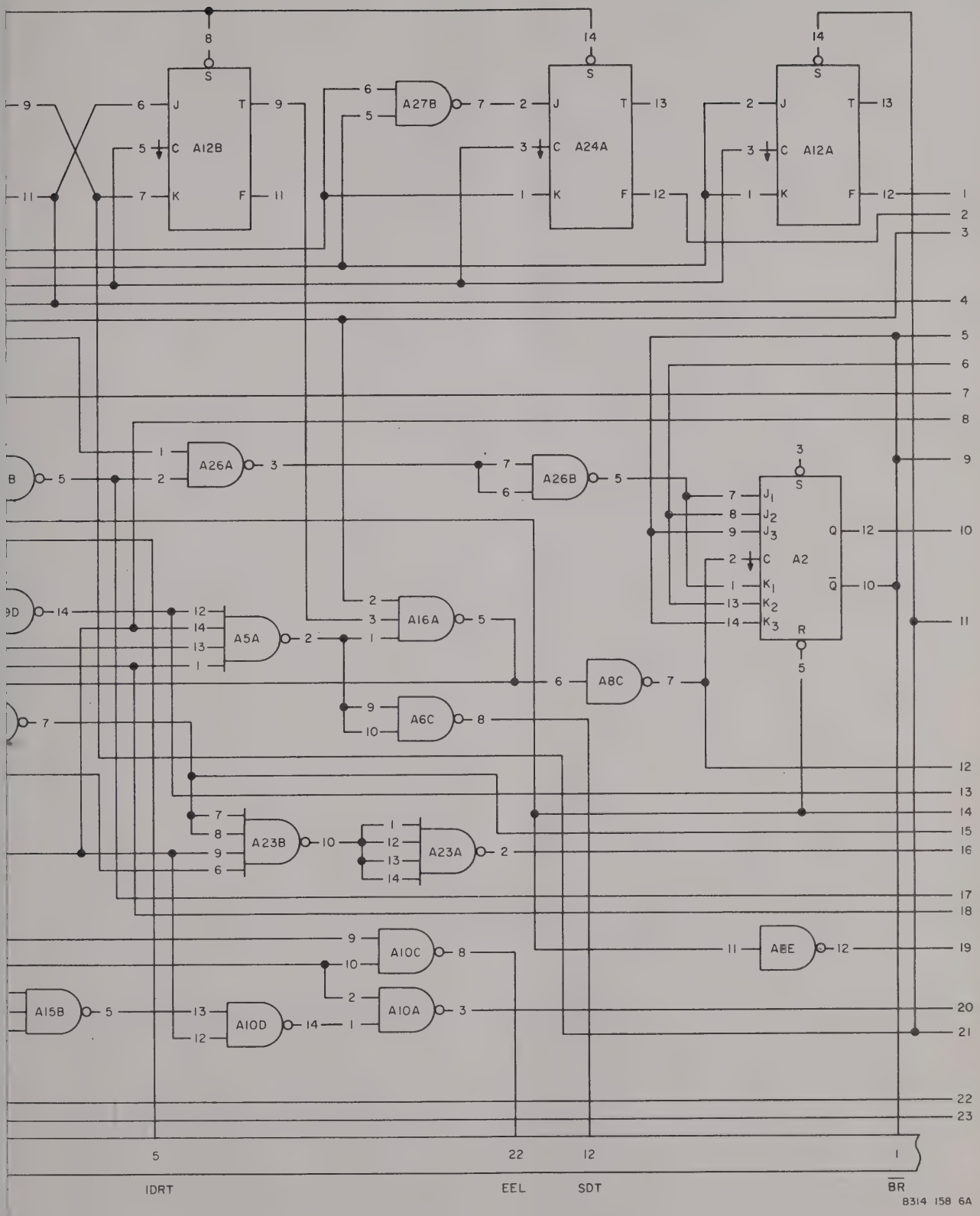
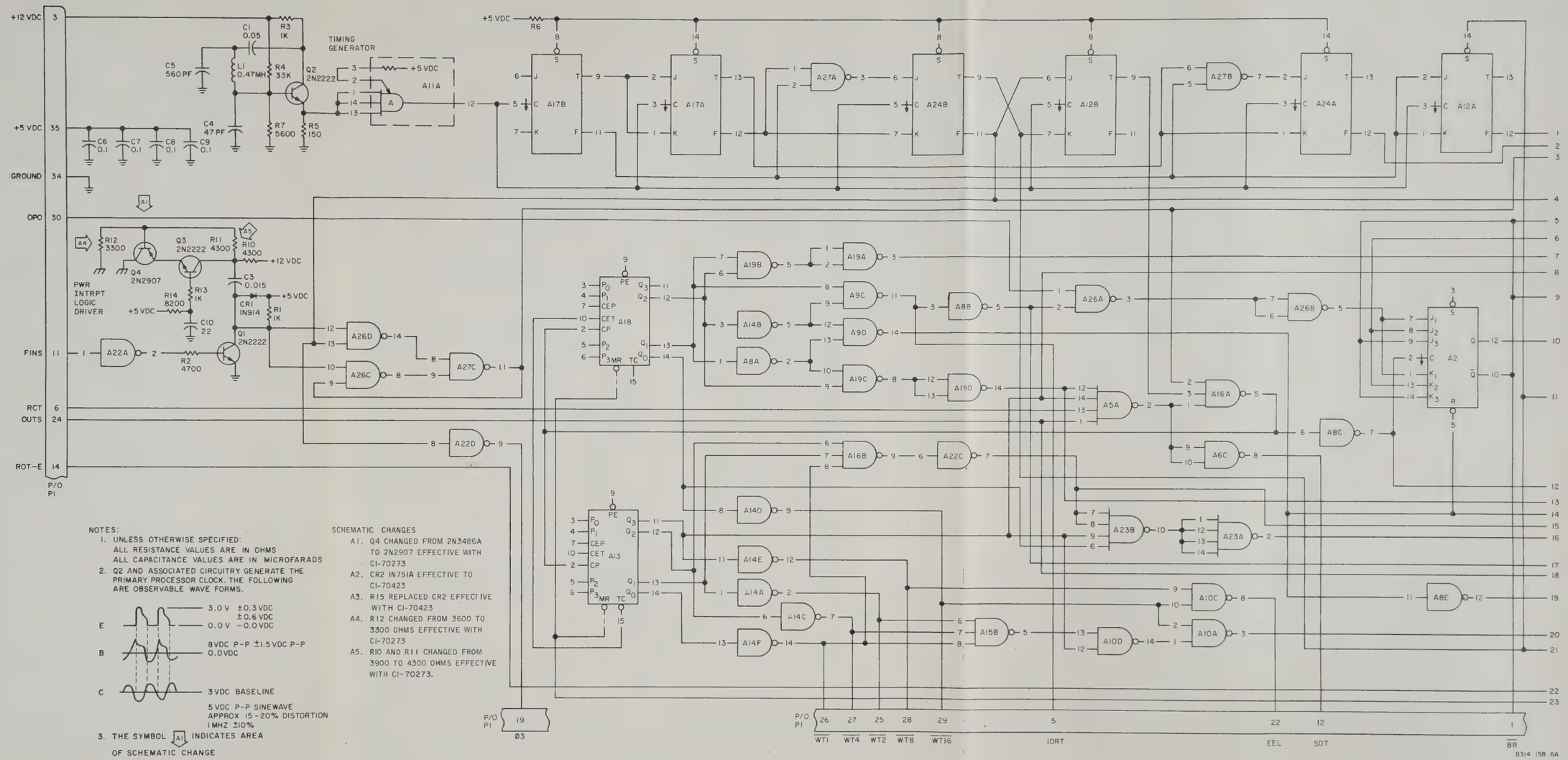


Figure 7-10. Processor Card, Detailed Logic Diagram (Sheet 1 of 2)



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE IN OHMS
   ALL CAPACITANCE VALUES ARE IN MICROFARADS
2. Q2 AND ASSOCIATED CIRCUITRY GENERATE THE PRIMARY PROCESSOR CLOCK. THE FOLLOWING ARE OBSERVABLE WAVE FORMS.

3. THE SYMBOL A1 INDICATES AREA OF SCHEMATIC CHANGE

SCHEMATIC CHANGES

A1. Q4 CHANGED FROM 2N3486A TO 2N2907 EFFECTIVE WITH CI-70273

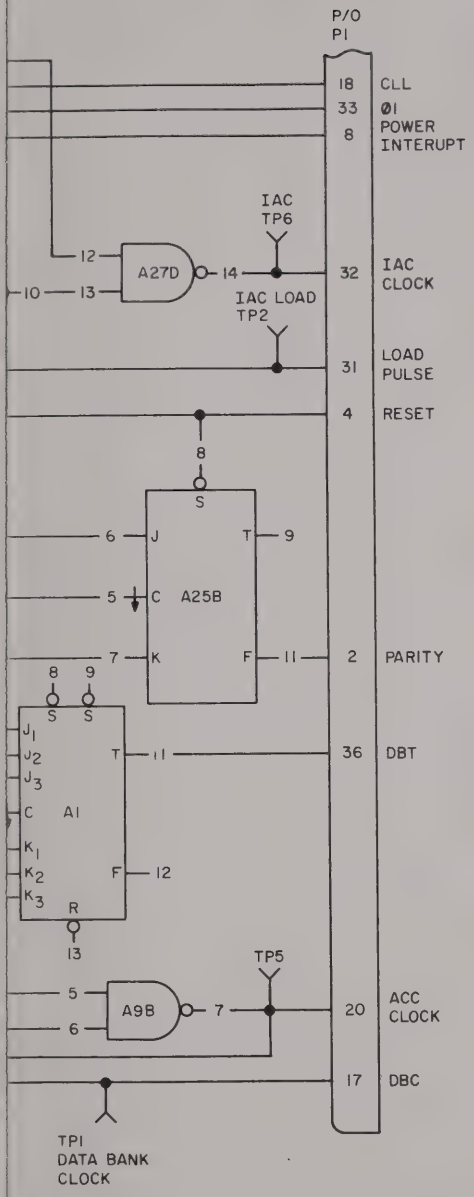
A2. CR2 IN751A EFFECTIVE TO CI-70423

A3. R15 REPLACED CR2 EFFECTIVE WITH CI-70423

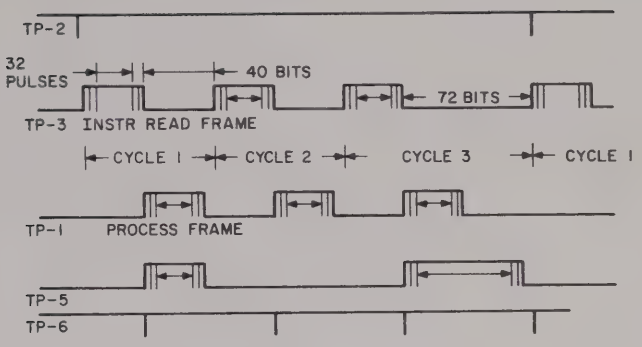
A4. R12 CHANGED FROM 3600 TO 3300 OHMS EFFECTIVE WITH CI-70273

A5. R10 AND R11 CHANGED FROM 3900 TO 4300 OHMS EFFECTIVE WITH CI-70273.

Figure 7-10. Processor Card, Detailed Logic Diagram (Sheet 1 of 2)



WAVEFORM CHART



TRANSISTOR VOLTAGE TABLE

Q NO	EMITTER	BASE	COLLECTOR
Q1	0V	0.2V +0.25V -0.2V	5V
Q2	SEE NOTE 2		
Q3	1.4V±	2V +0.24	1.7V±0.3V
Q4	1+4V±	0.7V ±0.1V	0V

INTEGRATED CIRCUITS TABLE

REFERENCE DES	TYPE
A13, A18	FC9316
A4, A15	SN54L10
A5, A23	SN54L20
A16	SG191
A12, A17, A24, A25	SF101
A11	SG80
A2	SN54L72
A21, A1	SF51
A8, A14, A22	RG371
A9	SG140
A27	SG141
A3, A6, A7, A10, A19, A20, A26	SN54L00

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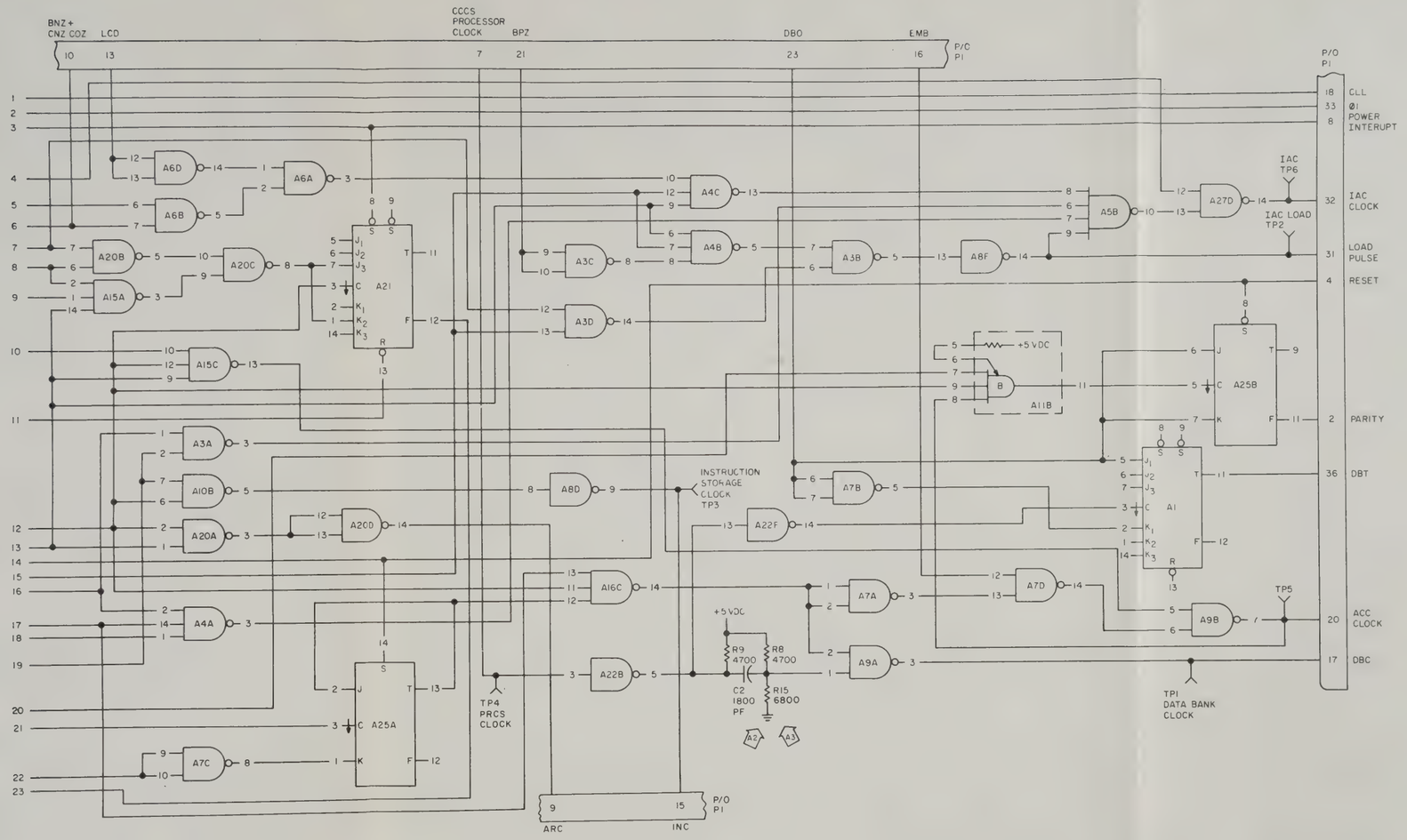
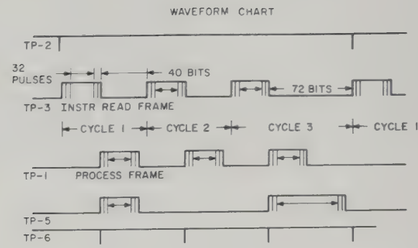
Figure 7-10. Processor Card, Detailed Logic Diagram (Sheet 2 of 2)





TRANSISTOR VOLTAGE TABLE

Q NO	EMITTER	BASE	COLLECTOR
Q1	0V	0.2V	+0.25V −0.2V	5V
Q2	SEE NOTE 2		
Q3	1.4V±	2V +0.24	1.7V±0.3V
Q4	1+4V ±	0.7V ±0.1V	0V

INTEGRATED CIRCUITS TABLE

REFERENCE DES	TYPE
A13, A18	FC93I6
A4, A15	SN54L10
A5, A23	SN54L20
A16	SGI9I
A12, A17, A24, A25	SFI0I
A11	SG80
A2	SN54L72
A21, A1	SF5I
A8, A14, A22	RG37I
A9	SGI40
A27	SGI4I
A3, A6, A7, A10, A19, A20, A26	SN54L00

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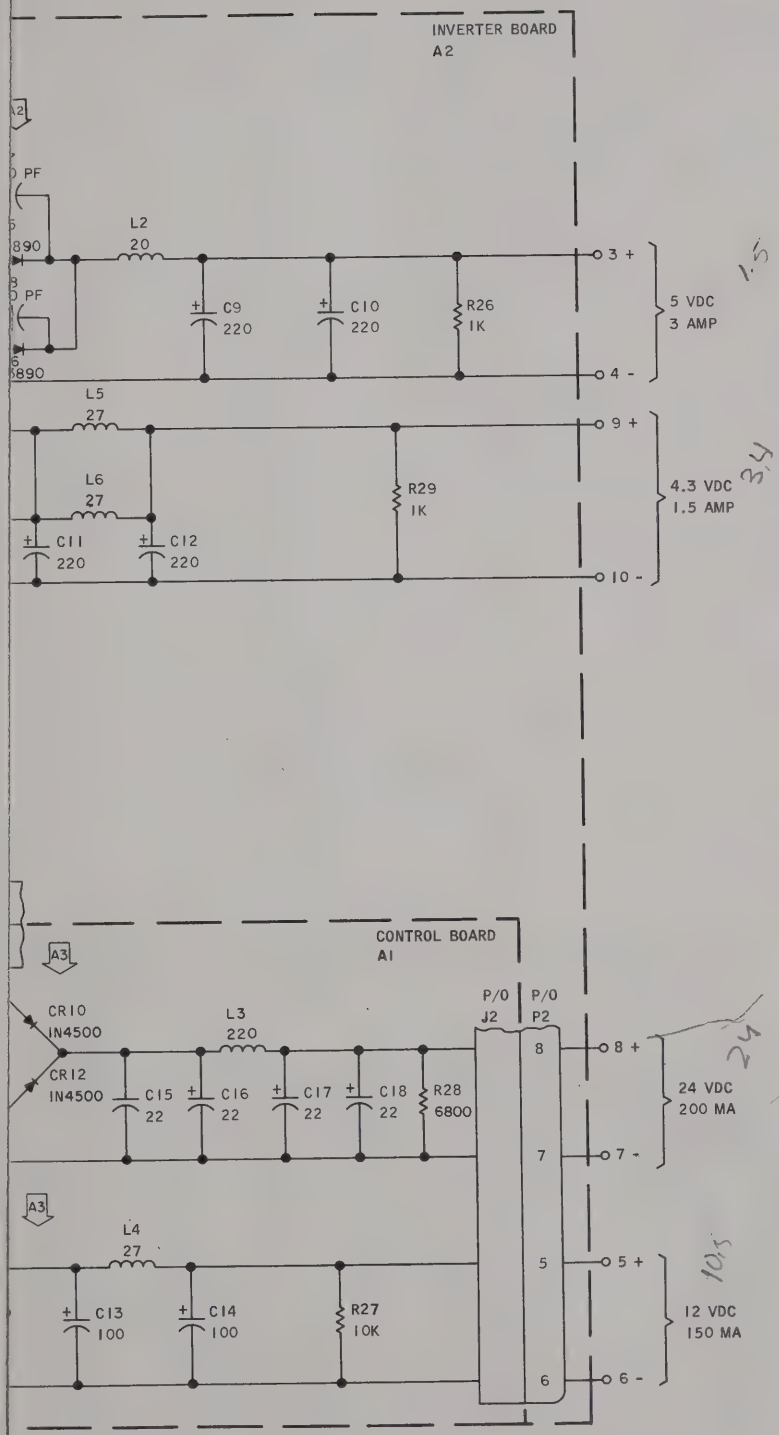
Figure 7-10. Processor Card, Detailed Logic Diagram (Sheet 2 of 2)



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE IN OHMS
   ALL CAPACITANCE VALUES ARE IN MICROFARADS
   ALL INDUCTANCE VALUES ARE IN MICROHENRYS
2. R24 AND L1 ARE CHASSIS MOUNTED, CR24 IS MOUNTED ON L1 TERMINALS
3. VOLTAGES AND WAVEFORMS SHOWN ARE TYPICAL WITH FULL LOAD AND 120 VAC 60 HZ INPUT VOLTAGE. ALL VOLTAGES ARE REFERENCED TO PIN 3 OF P1

VOLTAGE TABLE

TRANSISTOR	EMITTER	BASE	COLLECTOR
Q1	0V	-2.5V	SEE DIAG
Q2	0V	-2.5V	SEE DIAG
Q3	(CATHODE) -0.5V	(GATE) -0.5V	(ANODE) +150V
Q4	+6.4V	+5.8V	0V
Q5	+6.4V	+5.9V	-0.5V
Q6	-0.5V	-1.1V	-1.1V
Q7	-1.0V	-1.1V	-12V
Q8	-12V	-12V	-1.8V
Q9	-6.4V	-5.8V	0V
Q10	-6.4V	-5.8V	-1.8V
Q11	-2.5V	-1.8V	-1V

4. THE SYMBOL [A1] INDICATES AREA OF SCHEMATIC CHANGE.

SCHEMATIC CHANGES:

A1. R29 ADDED TO CONTROL BOARD A1 EFFECTIVE WITH CI-72263.
A2. C27, C28, C29, AND C30 ADDED TO INVERTER BOARD A2 EFFECTIVE WITH CI-72283.
A3. CR9 THRU CR16 CHANGED FROM IN691 TO IN4500 EFFECTIVE WITH REV J.

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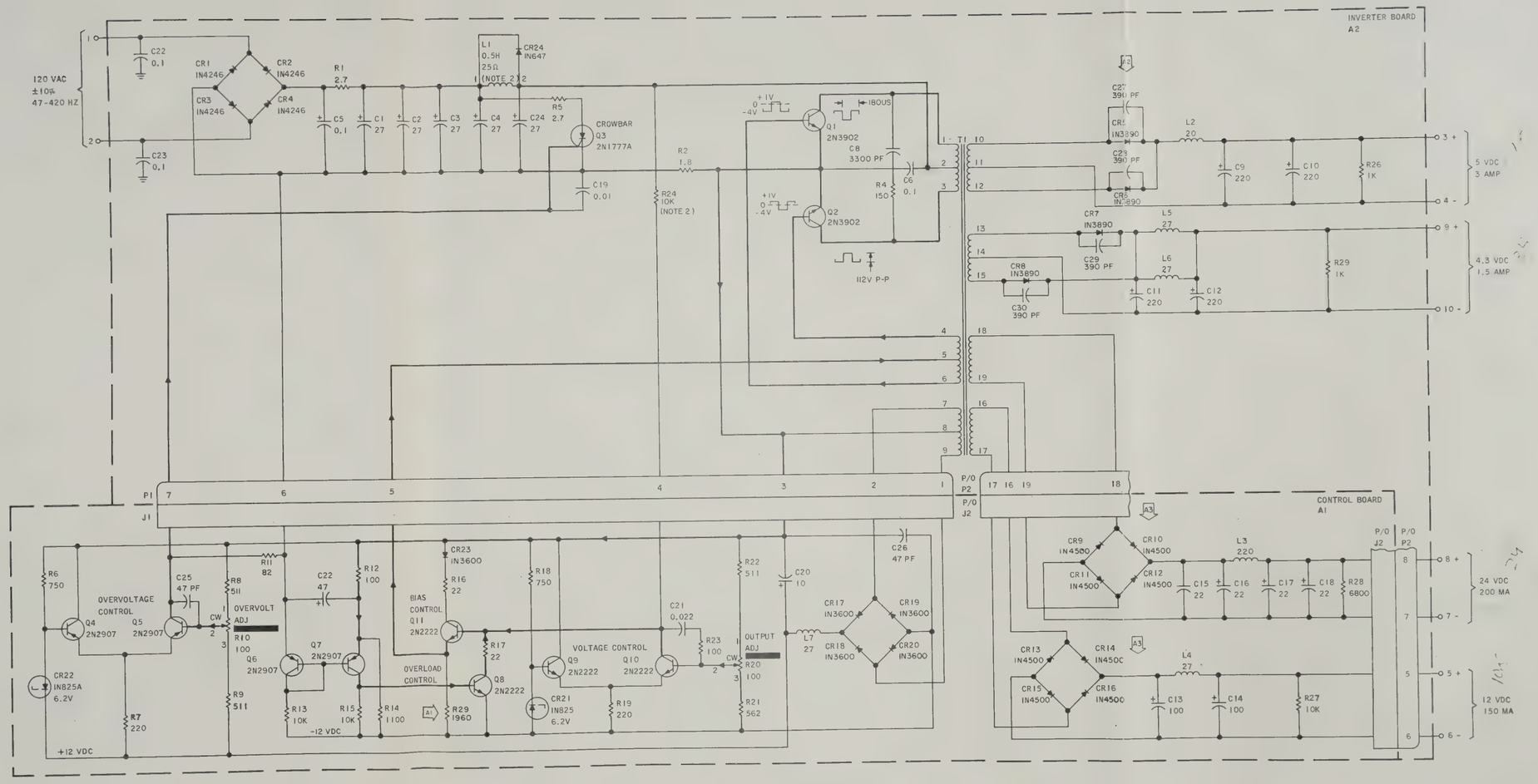
Figure 7-11. Transmit and Receive Control Head Power Supply, Schematic Diagram



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
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   ALL CAPACITANCE VALUES ARE IN MICROFARADS
   ALL INDUCTANCE VALUES ARE IN MICROHENRYS
2. R24 AND L1 ARE CHASSIS MOUNTED, CR24 IS MOUNTED ON L1 TERMINALS
3. VOLTAGES AND WAVEFORMS SHOWN ARE TYPICAL WITH FULL LOAD AND 120 VAC 60 HZ INPUT VOLTAGE. ALL VOLTAGES ARE REFERENCED TO PIN 3 OF P1

VOLTAGE TABLE

TRANSISTOR	EMITTER	BASE	COLLECTOR
Q1	0V	-2.5V	SEE DIAG
Q2	0V	-2.5V	SEE DIAG
Q3	(CATHODE) -0.5V	(GATE) -0.5V	(ANODE) +150V
Q4	+6.4V	+5.8V	0V
Q5	+6.4V	+5.9V	-0.5V
Q6	-0.5V	-1.1V	-1.1V
Q7	-1.0V	-1.1V	-12V
Q8	-12V	-12V	-1.8V
Q9	-6.4V	-5.8V	0V
Q10	-6.4V	-5.8V	-1.8V
Q11	-2.5V	-1.8V	-1V

4. THE SYMBOL A1 INDICATES AREA OF SCHEMATIC CHANGE.

SCHEMATIC CHANGES:
A1. R29 ADDED TO CONTROL BOARD A1 EFFECTIVE WITH CI-72263.
A2. C27, C28, C29, AND C30 ADDED TO INVERTER BOARD A2 EFFECTIVE WITH CI-72283.
A3. CR9 THRU CR16 CHANGED FROM IN691 TO IN4500 EFFECTIVE WITH REV J.

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Figure 7-11. Transmit and Receive Control Head Power Supply, Schematic Diagram

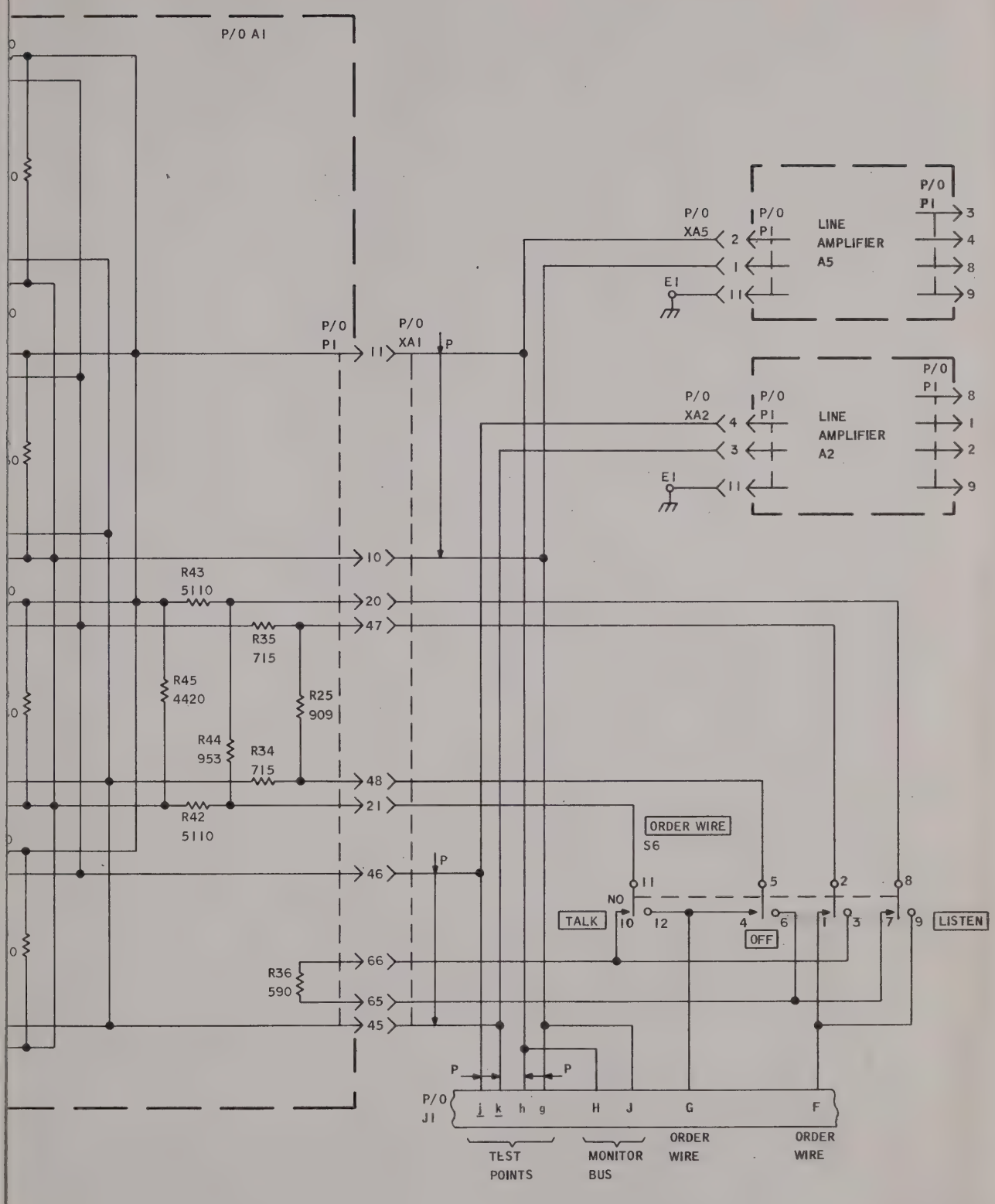

Figure 7-12. Audio Control Unit, Schematic Diagram (Sheet 1 of 2)

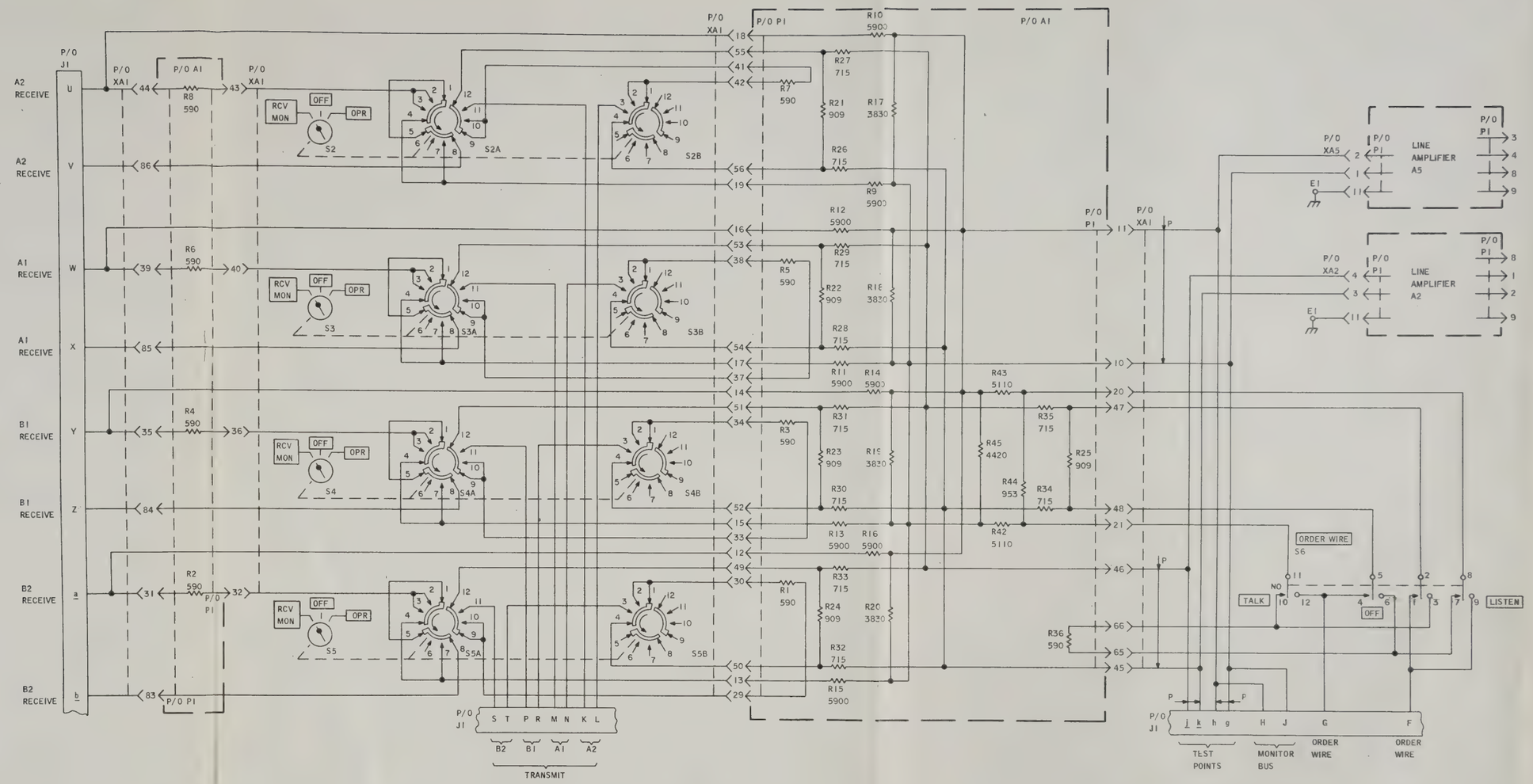

Figure 7-12. Audio Control Unit, Schematic Diagram (Sheet 1 of 2)

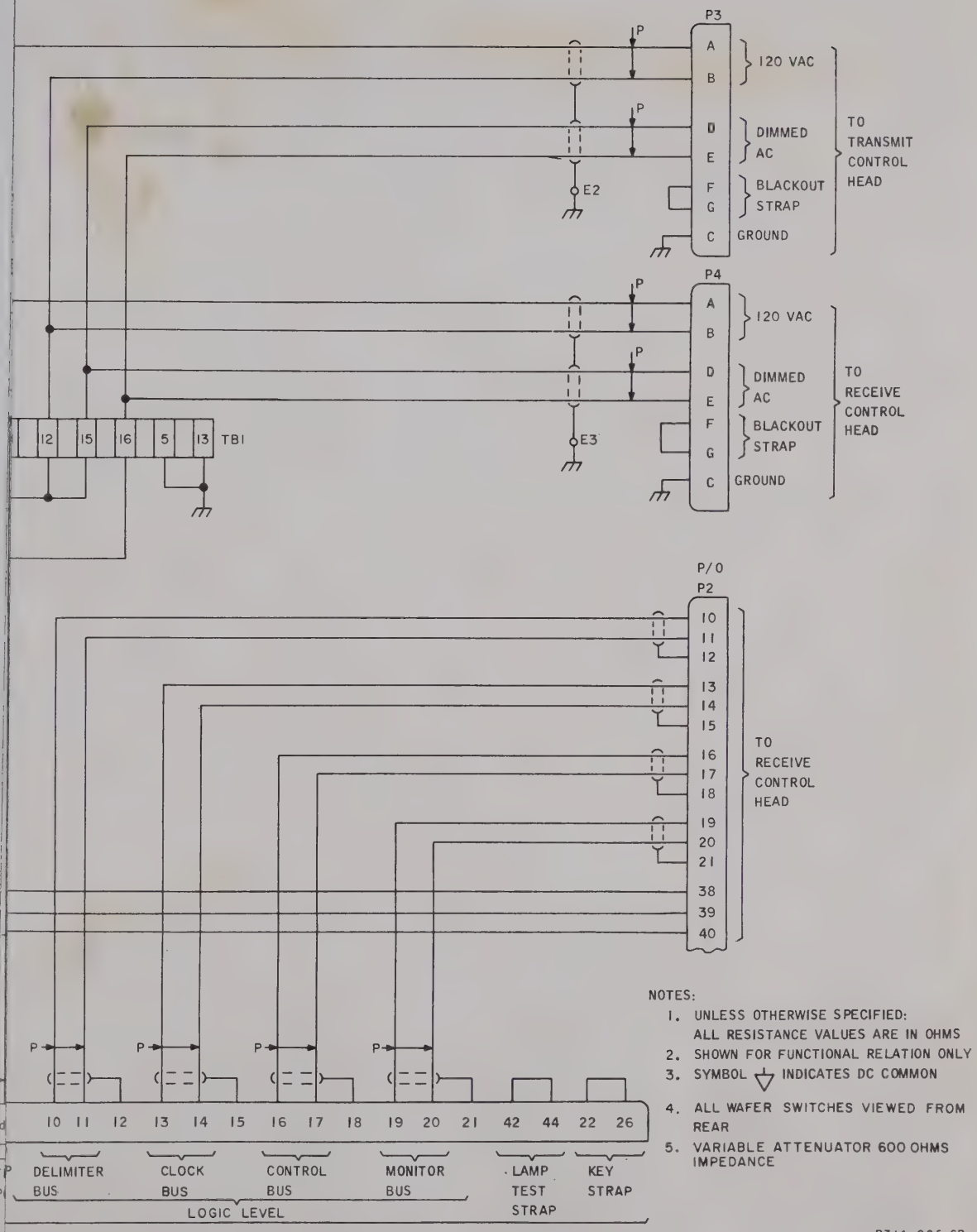

Figure 7-12. Audio Control Unit, Schematic Diagram (Sheet 2 of 2)

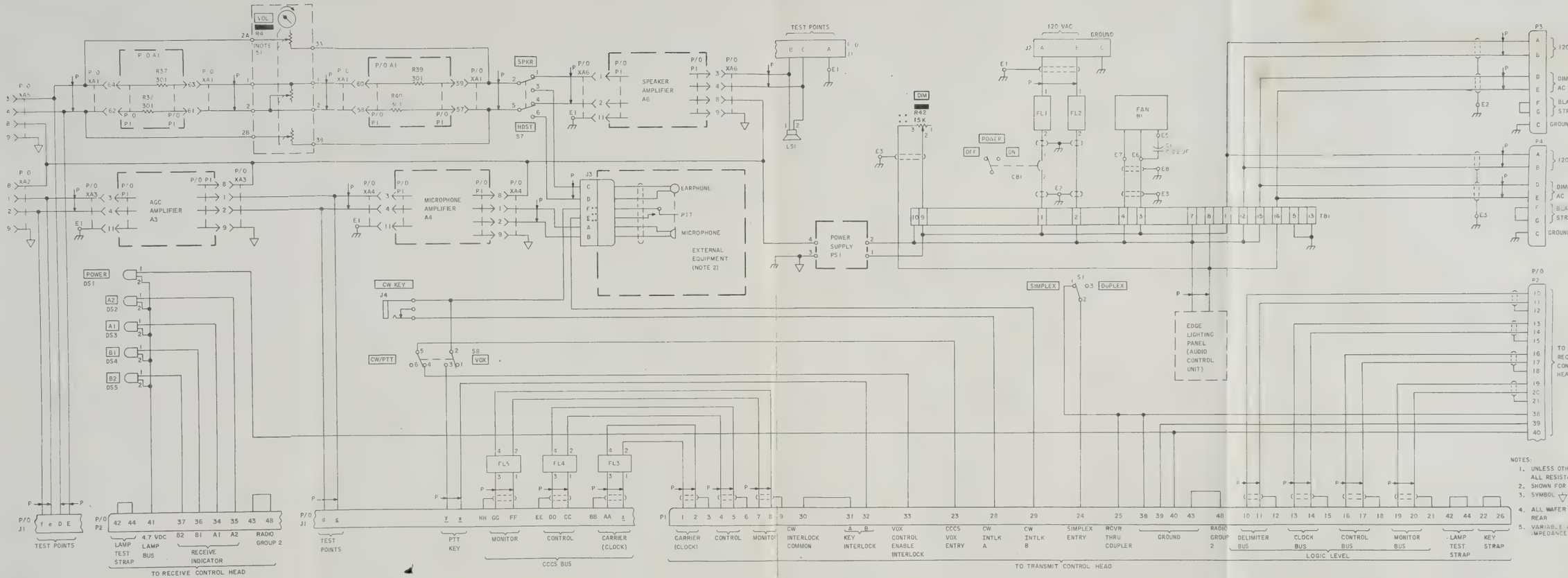

Figure 7-12. Audio Control Unit, Schematic Diagram (Sheet 2 of 2)

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